INTERNATIONAL JOURNAL of RENEWABLE ENERGY RESEARCH
S. A. M. Abdelwahab et al., Vol.16, No.1, March, 2026

Theoretical and Experimental Investigation of Bi-directional Hybrid Fault Current Limiter for HVDC System Based on Superconducting Material

Saad A. Mohamed Abdelwahab*‡, Hossam E. Mostafa Attia*, S. Hasan **, Ibrahim Shoaaib***, ****, A.M. Hamada***, ****

* Department of Electrical, Faculty of Technology and Education, Suez University, P.O.Box: 43221, Suez, Egypt.

** Electrical Engineering Department, Faculty of Engineering, Helwan University, Helwan, Egypt.

***Electrical Department, Faculty of Technological, Ministry of Higher Education, Alex., Egypt.

****Railway Department, Faculty of Industrial and Energy Technology, Borg El-Arab Technological, Alex., Egypt

(Saad.Abdelwahab@suezuniv.edu.eg, hossam.attia@ind.suezuni.edu.eg, ahsaady500@gmail.com, Ibrahimshoaaib@yahoo.com, abdallahmhe@yahoo.com)

‡Corresponding Author; Saad A. Mohamed Abdelwahab; 43221
Tel: +201096250375, Saad.Abdelwahab@suezuniv.edu.eg

Received: 28.01.2024 Accepted:27.02.2024

Abstract- This investigation explores an innovative topology for a bi-directional ultra-fast hybrid fault current limiter (UFHFCL) tailored for High Voltage Direct Current (HVDC) systems, integrating advanced superconducting materials. Theoretical analyses are employed to clarify the design principles and operational characteristics of the proposed HFCL, emphasizing its bidirectional fault current limiting capabilities. The strategy revolves around a UFHFCL that combines the advantages of a high-frequency transformer and a superconducting fault current limiter, designed to function as an exceedingly swift short-circuit protection method, limiting fault currents to safe levels within microseconds. The proposed approach offers a range of advantages, including heightened system reliability, minimized downtime, reduced losses, increased safety for personnel and equipment, and cost savings in the protection system. Rigorous testing of the strategy is conducted through simulations and experiments. Multiple simulation studies evaluate the UFHFCL's performance in HVDC systems, analyzing its behavior across various fault scenarios, considering factors like fault current magnitude, duration, and system parameters. Comprehensive insights into performance indicators such as fault current reduction, response time, voltage drop, energy dissipation, and system stability are gained through simulations. Experimental results unequivocally validate the UFHFCL's effectiveness in curtailing fault currents and ensuring industrial system protection. A scaled prototype of the proposed HFCL is employed for experimental validations, assessing its capability to limit fault currents bidirectionally within an HVDC system. This study aims to bridge the theoretical predictions and real-world performance, offering valuable insights into the practical application of bi-directional HFCLs to enhance the reliability and safety of HVDC systems.

Keywords HVDC, DC distribution networks, ultra-fast hybrid fault current limiter, SFCL, mechanical circuit breaker.

1. Introduction

The critical issue of limiting DC fault currents in DC distribution networks, especially HVDC High Voltage DC systems and the challenges faced in implementing them practically. A significant challenge in HVDC grids is the requirement for a high-speed DC-side protection system capable of promptly detecting, identifying, and interrupting DC faults. To address this challenge, a novel architecture for a proactive UFHFCL is proposed. The UFHFCL aims to effectively isolate DC faults in HVDC grids, thereby enhancing the reliability and overall performance of these grids. The study addresses a critical need in the electric power industry by proposing an innovative solution to enhance the stability, reliability, and safety of HVDC systems. By introducing the concept of UFHFCL tailored for HVDC systems, the study offers potential benefits such as heightened system reliability, minimized downtime, reduced losses, increased safety for personnel and equipment, and cost savings in the protection system. The paper also addresses the suggested topology's simulation-based analysis to validate its efficiency and efficacy in reducing interruption time, enhancing breaking current capability.

The electricity system's transmission equipment is being asked to perform at higher standards. Therefore, interested individuals must consider ways to increase the stability and dependability of power. Transmission equipment is becoming the electric power industry's development trend [1]. Protecting against overcurrent in DC systems poses greater challenges compared to AC systems due to fundamental differences in the design and operation of DC circuit breakers [2]. Unlike AC systems, DC circuits lack a natural zero crossing point [1, 3, 4]. HVDC circuit breakers have traditionally been utilized to interrupt fault currents [5]. However, their response time has proven to be too slow for the demands of HVDC networks, typically in the range of several tens of milliseconds [6]. Although semiconductor-based breakers can meet the speed requirements, they tend to result in significant on-state losses. One commonly used design is the DC Circuit Breaker (DCCB), which is engineered to open the circuit upon detecting a fault, thereby restricting the flow of fault current. However, the performance of DC-CBs can be limited by factors such as the high cost and complexity of the breaker, slow response time, and high-power loss during operation [7]. A DC hybrid CB is designed to interrupt or limit DC current. This breaker combines the benefits of both mechanical and power electronics-based CBs. It comprises a mechanical switch and a power electronics switch connected in series. The mechanical switch interrupts the normal current flow, while the power electronics switch restricts the fault current [8 -11]

The utilization of superconducting fault current limiters (SFCLs) takes advantage of the unique properties exhibited by superconducting materials. Superconducting materials, such as superconducting magnetic coils (SMCs), possess characteristics of zero-resistance and perfect diamagnetism. Consequently, during normal operation of the HVDC grid, the SFCL exhibits low impedance. However, when the SFCL detects a sudden increase in current, it rapidly transitions into a high impedance state [12]. Certain designs of SFCLs have demonstrated reliable performance in low- and medium-voltage installations [13]. The breaker's design marks a notable progress in achieving a high-speed and low-loss HVDC circuit breaker. This hybrid design successfully eliminates on-state losses and enables exceptionally rapid operation [14].

Previous studies have presented the incorporation of the hybrid CB model, derived from this design, into a time-domain simulation tool. These works have explored the implementation with varying degrees of complexity [13, 15, 16]. In one study [17], hybrid circuit breaker model was assessed using a simplified test system configuration. The study aimed to assess the effectiveness of various HVDC breaker designs, including the hybrid model, in protecting HVDC multiterminal systems. Expanding on previous research, this study extends its scope by examining a more complex HVDC system configuration. The comprehensive analysis encompasses multiple converters, transmission lines, and diverse system parameters, such as fault location and fault resistance. Evaluation of different breaker designs is based on criteria such as current interruption capability, fault clearing time, and stress on the converter valves [14,16]. The hybrid design emerges as a promising choice for HVDC multiterminal systems, demonstrating strong performance in terms of current interruption and minimal stress on the converter valves. The findings from this study offer valuable insights for the design and operation of HVDC systems, especially those with multiple terminals [18].

Another proposed design for DC current interruption or limitation is a superconducting DC fault current limiter [19]. This device employs SMCs to restrict fault current by establishing a low-resistance pathway for the current. Upon detecting a fault current, the superconductor transitions into a normal conducting state, thereby restricting the current flow. After the fault current subsides, the superconductor reverts to its superconducting state, enabling the resumption of normal current flow [20]

In this paper, theoretical and experimental innovative UFHFCL is introduced, which combines the advantages of superconductor material (SCM) with HVDC systems. The primary purpose of the study is to investigate an innovative topology for a bi-directional ultra-fast hybrid fault current limiter (UFHFCL) tailored for High Voltage Direct Current (HVDC) systems. This investigation aims to address the critical issue of limiting DC fault currents in HVDC distribution networks, particularly focusing on HVDC systems, which pose unique challenges compared to AC systems due to the absence of a natural zero crossing point.

The paper investigates the impact of the UFHFCL under various conditions in a DC system. The hybrid CBS design is a promising technology that has the potential to revolutionize the way HVDC systems are protected. It offers several advantages over traditional CB designs, and it is well-suited for the demands of meshed HVDC systems. A novel technique is proposed in this study to address the issue of over-voltage sensitivity in the activation of integrated gate-commutated thyristors (IGCTs). The technique involves the implementation of a capacitive current branch, which effectively dissipates the electromagnetic energy from the faulty line. By doing so, the technique effectively reduces the magnitude of over-voltage experienced during the activation process of the IGCTs. The control strategy is extremely straightforward. Piecewise linear electrical circuit simulation program (PLECS) with a simple network is used, the fault mode is simulated under various conditions. The simulation results clearly exhibit the effectiveness of incorporating UFHFCL into the system in suppressing over-voltages. Initially, the study was conducted without considering the current limiting reactor (CLR)in the breaker model. However, the final section of this work focuses on analyzing the impact of the CLR on over-currents and over-voltages resulting from faults. The findings of the study provide valuable insights for the design and operation of HVDC systems, especially those with multiple terminals, contributing to the advancement of transmission equipment in the electric power industry. Overall, the theoretical and experimental results provide evidence of the UFHFCL's efficacy in limiting fault currents and enhancing power system reliability.

This paper is structured as follows: Section 2 discusses the fundamental design and operation principles of the hybrid circuit breaker. Section 3 presents the hybrid HVDC circuit breaker model. It summarizes the key characteristics of the breaker model and justifies the need for a simplified representation. A simplified breaker model is proposed in this part, to look at the interaction between the test system and the breaker during breaker operation. Section 4 presents the simulation test of proposed scheme using PLECS program. The operation of the breaker after a fault and the transients that result from it are both thoroughly examined. It includes information about the test system used in this study, case studies conducted using a lattice diagram approach, and a sensitivity analysis considering over-current's and over-voltage. In section 5 experimental work and results of the operation of the UFHFCL are presented. Section 6: The conclusion of the paper is provided.

2. UFHFCL Configuration and Fundamental Principle of Operation

The performance and efficacy of the hybrid fault current limiters were assessed over the course of the last two years by the researchers using a combination of simulated laboratory tests, mathematical modelling, and simulation. The main issues requiring resolution in the hybrid circuit breaker design pertain to the current commutation processes involving the bypass switch and the superconducting current bypass, along with considerations for the discharge resistor [21]. timing for cutting off the basic path, coordination between the basic path and the commutation path, and Operational limitations. [7,11,13].

Research has increased the usage of metal-oxide varistors (MOVs) in standard techniques for lowering recovery voltage in DC systems. MOVs have nonlinear current-voltage properties and are voltage-dependent resistors. By restraining excessive voltage levels and rerouting transient currents to save delicate components, they serve as surge suppressors. [22-24]. The MOV quickly changes from high resistance to low resistance when faced with a voltage surge. This fast response allows it to absorb excess energy and limit downstream voltage. However, it has a limited lifespan and gradually deteriorates due to voltage surges. Extreme surge conditions can cause thermal runaway, and the MOV's properties determine the voltage clamping level, which may not be properly regulated. In this research, we aim to provide a balanced understanding by discussing potential barriers or challenges associated with hybrid technology. These include complexity, cost, scalability, limited research and development, and operational limitations [25].

The article briefly mentions the current and timing switching operations. However, more details on potential limitations or transient behavior, such as voltage spikes or current oscillations during the switching process, will provide a more comprehensive understanding of the technology. Including a discussion of these potential drawbacks or limitations would provide a more balanced perspective of the hybrid technology used in shielding superconducting magnets and help readers understand the challenges and considerations associated with its implementation. A hybrid current limiter has been proposed that combines the properties and advantages of superconducting conductors as well as the properties of ultrafast electronic elements. using the electronic path to reduce recovery voltage.

2.1. Arrangement of Proposed UFHFCL

Figure 1 illustrates the configuration of the hybrid HVDC circuit breaker, employing a fault current limiter topology. This topology involves the shunt connection of the main branch, consisting of an auxiliary branch and a current-limiting branch.

Under normal conditions, the ultrafast disconnector (UFD) or main mechanical switch within the main branch remains closed, allowing the main current to flow. Consequently, the on-state power loss is restricted to a level similar to that of a conventional mechanical circuit breaker (MCB). Additionally, a load commutation element, such as a superconducting coil, can be employed to replace the copper coil in the DC reactor to minimize losses during normal operation.

The auxiliary sub-path incorporates semiconductors that offer improved performance characteristics for current control. Due to their high-performance speed, two insulated-gate bipolar transistors (IGBT) are employed to lessen the creation of an arc during the opening of a mechanical switch in both directions, therefore, due to the occurrence of the interruption process of the fault current, this path can be called an arc less hybrid circuit breaker with semiconductor in main current limiting path. To minimize power loss during normal operation, a load commutation element, such as a superconducting coil, can be employed to replace the copper coil in the DC reactor.

This substitution helps reduce power loss and improve the efficiency of the system. The auxiliary sub-path incorporates semiconductors that offer improved performance characteristics for current control. Specifically, two IGBTs are employed to minimize the creation of an arc during the opening of a mechanical switch in both directions. This feature makes the circuit breaker an arc-less formation with semiconductors in the main current-limiting path. Overall, the configuration presented in Fig. 1 combines the advantages of mechanical switches and semiconductor devices to achieve efficient and reliable fault current limitation in HVDC grids.

The current-limiting branch of the hybrid HVDC circuit breaker consists of an inductor, capacitor, and a thyristor valve connected to the terminals. This branch utilizes a single-phase uncontrolled bridge-type diode scheme (D1-D4) based on self-turn-off devices like IGBTs. It incorporates a pre-charged capacitor (C_{lim}) and an inductance (L_{Lim}) to enhance its functionality. In the DC grid, the bridge-type configuration comprises a diode bridge with four series diode groups (D1-D4). Furthermore, there is a series connection of a DC reactor and a DC biased power supply between the shared cathode point of D1 and D3, as well as the shared anode point of D2 and D4. This setup enables bidirectional current flow and provides the capability for current limitation, as illustrated in Fig. 1. By integrating these components and the bridge-type configuration, the presented UFHFCL design achieves effective current limitation and enables bidirectional current flow, as demonstrated in Fig. 1.

2.2. Principles of Operation

During normal operation, the hybrid switch (typically an IGCT) in the second path of the circuit is in a blocking state, and the diodes are reverse-biased. The capacitor is charged to a voltage slightly lower than the HV system voltage. During normal operation, the main contact of the hybrid HVDC circuit breaker is closed, allowing the line current to pass through the primary branch, which consists of the SCM and the MCB. The primary branch has a low conduction resistance, enabling efficient current flow shown Fig.2 (a). In the event of a fault, the current is diverted to the auxiliary branch, which is made up of series-connected semiconductor cells. Fig.2 (b). The cells within the hybrid HVDC circuit breaker play a crucial role in redirecting the fault current and protecting the MCB from excessive voltage. These cells quickly open to create a new current path, ensuring that the increasing voltage across the breaker is mitigated. At the same time, the UFD opens as soon as the auxiliary branch no longer carries current. A residual current breaker safeguards the solid-state banks from thermal overload by disconnecting the faulty line or cable from the HVDC grid, interrupting the residual arrester current. In the event of a detected fault, the semiconductor branch is activated (if not already active), and the commutating element is triggered to facilitate current commutation and interruption. As the current in the isolating switch decreases, the current in the semiconductor branch begins to rise. The control circuit monitors the short circuit current continually and compares it to a predefined threshold. Once the short circuit current surpasses this threshold, the control circuit sends a signal to the electrodynamic drive, causing the main contact to open and effectively interrupt the fault current. Upon opening of the main contact, the fault current is directed towards the auxiliary solid-state branch, and a signal is generated to activate the commutation thyristors, known as IGCT. This activation signal enables the fault current to pass through the current-limiting branch of the hybrid HVDC circuit breaker.

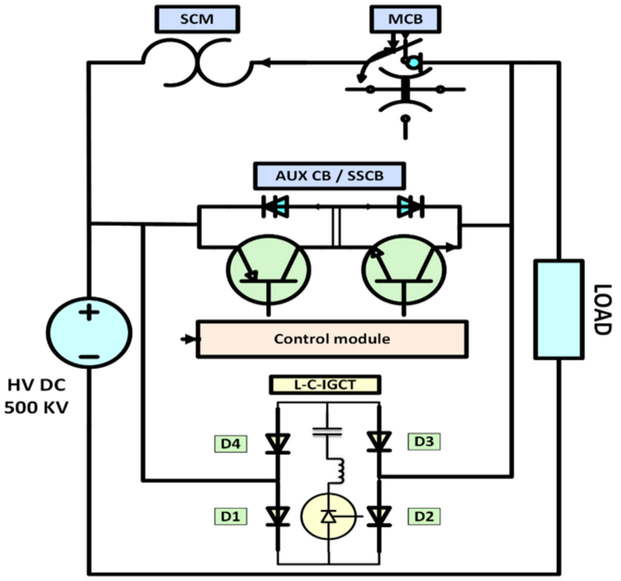
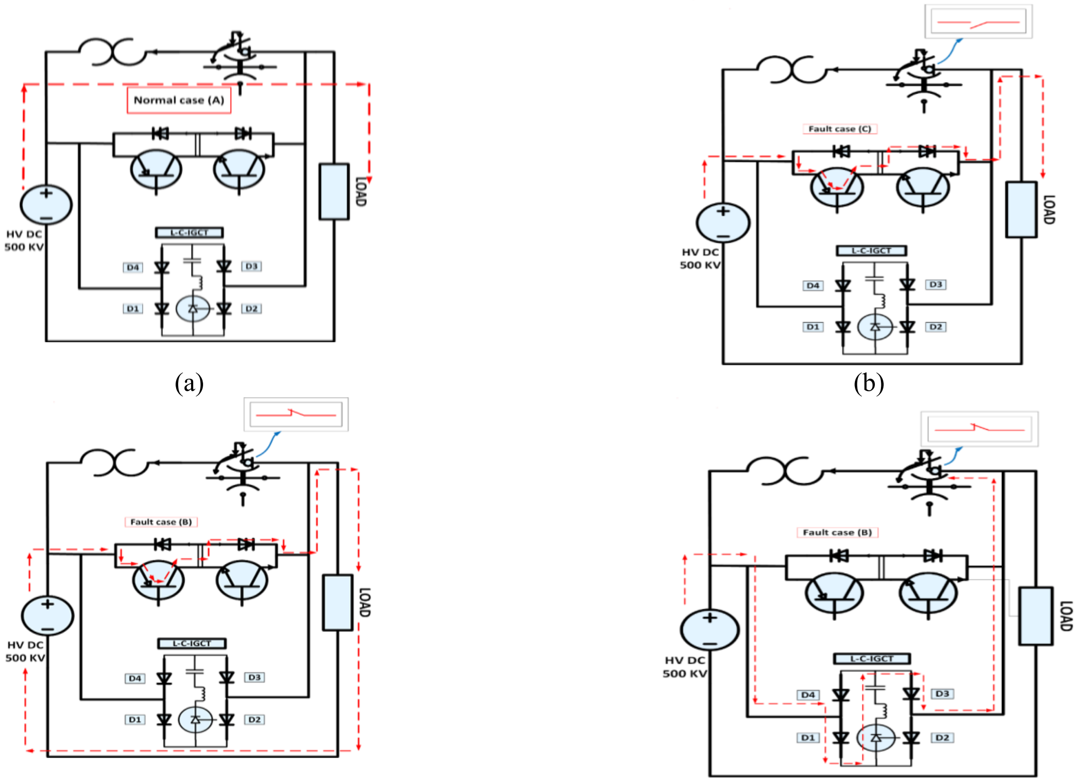


Fig. 1. Schematic circuit diagram of UFHFCL in DC system

The control scheme of the circuit breaker is specifically designed to accurately determine the direction of the fault current, particularly in cases where the short circuit current exceeds a predefined threshold, such as 20 kA, at a voltage of 500 kV. The IGCTs play a crucial role in the interruption process, relying on the control circuit's signal to ensure effective current commutation and interruption. For a visual representation of the circuit configuration and the involvement of IGCTs, specifically Fig. 1(c).

The combination of the IGCT and diodes in parallel creates a low-impedance path for the fault current, effectively limiting the current to a safe level. The presence of the capacitor ensures that the IGCT and diodes remain conducting until the fault current either decays naturally or until the main switch opens. In the situation where the fault current originates from the opposite terminal as shown in Fig. 2 (d), the sequence of events follows a similar pattern as described earlier. However, in this case, only the IGCT connected to the respective diodes (D2 and D4) will be triggered, allowing the fault current to be diverted through that particular path. The remaining components and operation of the circuit remain unchanged. In the event of a fault occurring on the other end of the circuit, the fault current will flow through diodes D2 and D4. This will cause the voltage across the commutation booster circuit to become negative. As a result, the IGCT in the commutation booster circuit will remain in a blocking state, preventing the fault current from flowing through that specific path. However, when the fault current reaches a specific level, the IGCT in the main branch is activated, offering a low-impedance route for the fault current. The mechanical switch doesn't require generating a high arc voltage during the commutation process since the main branch with the IGCT provides an alternative path for the fault current.

The diodes D1 and D3 in the auxiliary branch will be reverse-biased, and the capacitor will discharge through the commutation booster circuit, Therefore, in this scenario, only the IGCT in the branch will be triggered on, with the other diodes in the circuit providing an alternate path for the fault current. The inclusion of the commutation booster auxiliary branch in the hybrid circuit breaker design helps reduce the requirement for a high arc voltage across the mechanical switch. In traditional FCLs, MOVs or zinc oxide varistors are commonly used to mitigate the electric arc voltage that arises during switching operations. These varistors are nonlinear devices that exhibit high resistance at low voltages and low resistance at high voltages. By utilizing such varistors, the circuit can effectively limit the electric arc voltage and prevent it from reaching high levels, reducing the stress on the mechanical switch. This helps enhance the overall performance and longevity of the circuit breaker. When a fault occurs, the fault current generates a high voltage across the mechanical switch, causing an electric arc to form. This arc generates heat and can cause damage to the switch, as well as interfere with the proper functioning of the fault current limiter.



(a) (b)

(c) (d)

Fig. 2. (a) Normal case of operation, (b) fault case and close CB, (c) fault case and open CB, (d) fault case and current limiting path.

Figure 2 show the flowchart detailing the envisioned protection scheme. The varistors are used to reduce the voltage across the mechanical switch by absorbing the excess energy and dissipating it as heat. This helps to prevent the electric arc from forming and reduces the risk of damage to the switch. In this paper, ultra-fast semiconductor technology was used instead of traditional varistors to reduce the electric arc voltage. This technology uses ultra-fast switching devices such as IGBTs or silicon carbide devices to provide a low-impedance path for the fault current.

These devices have a much lower on-state resistance compared to traditional varistors, which means they can handle higher current levels without generating a high arc voltage. This, in turn, helps to reduce the voltage across the mechanical switch and prevent the formation of an electric arc. In addition, ultra-fast semiconductor technology provides faster switching speeds compared to traditional varistors, which helps to improve the overall performance of the fault current limiter. The faster switching speeds allow the fault current to be interrupted more quickly, which can help to minimize damage to the system and reduce downtime. Overall, the use of ultra-fast semiconductor technology instead of traditional varistors provides several advantages, including lower on-state resistance, faster switching speeds, and improved performance of the fault current limiter.

Effective coordination between the FCL and the DCCB is crucial for achieving optimal operation. The emphasis is particularly on minimizing the overall fault clearing time, often referred to as the isolation speed, of the DCCB. In the context of modular multi-level converters (MMC) based DC grids, the hybrid DCCB is considered a highly promising technique. When analyzing the performance of the FCL and DCCB and their coordination in real-world scenarios, it is important to acknowledge the complexity and time-consuming nature of creating a comprehensive representation of the hybrid circuit breaker design. The use of simplified models, as proposed in [26], can alleviate some of these challenges.

The proposed model in [27] introduces simplifications to represent the hybrid circuit breaker more efficiently. By treating IGBTs as ideal switches in parallel with their on-state loss resistance and parasitic inductance, their response to current commutation from the auxiliary branch can be mimicked using a single IGBT in series with combined resistances and inductances. The auxiliary branch can be depicted as a single ideal switch with a parallel diode and a parallel snubber circuit, capturing the essential behavior of the ideal switch without considering arc dynamics, effectively representing the FCL. For the main branch, additional simplification is possible by utilizing a single switch in series with the on-state loss resistor and parasitic inductance. These simplifications significantly enhance the manageability of the hybrid circuit breaker model, reducing computational complexity and the time needed for transient simulations. This approach enables researchers to assess the performance of the FCL and DCCB more efficiently, facilitating analysis and optimization in practical applications.

3. Simulation Part of Proposed Scheme

3.1. Optimum Parameters of UFHFCL Commutation Circuit

The optimal performance of the circuit relies significantly on determining the ideal values for the commutation circuit parameters. To derive these values, equations based on Kirchhoff's voltage law and Kirchhoff's current law are employed. These fundamental laws form the basis for analyzing and comprehending the circuit's behavior. Utilizing Kirchhoff's voltage law, which asserts that the sum of voltages in a closed loop is zero, and Kirchhoff's current law, which asserts that the sum of currents at any node is zero, a set of equations can be formulated. These equations consider the circuit's topology, its components, and their interconnections. The governing differential equations derived characterize the dynamic behavior of the circuit. Solving these equations allows us to identify the optimal values for the commutation circuit parameters, meeting the specified criteria for circuit performance.

These parameters may include resistances, inductances, capacitances, and other relevant characteristics. Through mathematical analysis and solution techniques, such as numerical methods or analytical approaches, the optimal values can be determined. The goal is to find parameter values that yield stable and efficient circuit operation, ensuring smooth commutation and reliable performance. By utilizing the principles of Kirchhoff's laws and the derived differential equations, engineers and researchers can effectively analyze, design, and optimize the commutation circuit parameters to achieve the desired behavior and performance of the circuit. It is important to note that the specific form of these equations and differential equations will depend on the circuit topology, components used, and the desired performance criteria. The process of deriving and solving these equations requires a thorough understanding of circuit theory and analysis techniques as shown in the flow chart shown in Fig. 3.

$$L\frac{d^2 i_2}{dt^2} + \frac{1}{C} i_2 + \frac{du_{\text{arc}}}{di_1}\frac{di_1}{dt} = 0 \qquad (1)$$

$$\mathrm{i_{dc}} = \mathrm{i_1} + \mathrm{i_2} + \mathrm{i_3} \qquad (2)$$

The calculation of the current on the main branch, denoted as i1, involves solving the governing differential equations obtained from Kirchhoff's voltage law and Kirchhoff's current law. The exact form of these equations and the solution method are contingent on the circuit's specific configuration and parameters. Detailed information, including the solution methodology and equations for determining the current on the main branch, can be found in [28]. It is recommended to refer to that specific reference for the accurate equations and solution technique.

$$i_1 = i_{dc}\left\{1 + e^{-(0.5L)(\,du_{arc}/di_1 t)}\sin\left(\sqrt{\frac{1}{LC}}\,t\right)\right\} \quad (3)$$

The charging process of the auxiliary path is characterized by a differential equation that dictates the rate of change of either the voltage or current in the auxiliary path. This equation may involve parameters such as the capacitance of the auxiliary capacitor, the resistance or impedance of the auxiliary path, and the initial conditions of the system. The charging process of the auxiliary path can be expressed in the following differential equation:

$$L_1 C_1 \frac{d^2 V_c}{dt^2} + V_c + L_2 C_1 \frac{d^2 V_c}{dt^2} + R_g C_1 \frac{dV_c}{dt} = U_{dc} \qquad (4)$$

Equation (4), which highlights a distinct relationship among the parameters in the innovative DC circuit breaker. Equation (4) models the behavior of the circuit breaker, incorporating the influence of various parameters on the voltage Vc across the circuit breaker terminals over time.

- L_1 and L_2 represent the inductances in the circuit.
- C_1 denotes the capacitance.
- R_g signifies the resistance.
- U_{dc} is the DC voltage applied across the circuit.

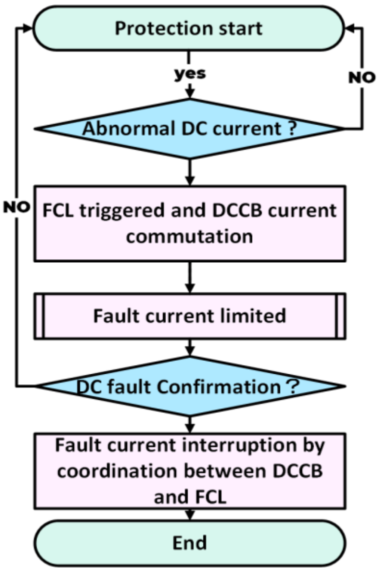


Fig. 3. The flowchart detailing the envisioned protection scheme

The equation captures the dynamics of the circuit breaker system, considering the effects of inductance, capacitance, resistance, and the applied DC voltage. The second derivatives $\frac{d^2 V_c}{dt^2}$ represent the rates of change of the voltage Vc with respect to time, while $\frac{dV_c}{dt}$ denotes the first derivative.

$$\frac{R_g}{2}\sqrt{\frac{C_1}{L_1 + L_2}} > 1 \qquad (5)$$

Alongside the initial conditions, Vc=0 and dVc/dt =0 at t = 0. The voltage on the capacitor is

$$V_c = U_{dc}\left(1 - A_1 e^{-\beta t}\sinh(\omega t + \varphi)\right) \qquad (6)$$

In (6), A1, β, and ω can be expressed as

$$A_1 = \sqrt{\frac{4(L_1+L_2)}{R_g^2 C_1 - 4(L_1+L_2)}}$$

$$\beta = \frac{R_g}{2(L_1+L_2)} \tag{7}$$

$$\omega = \frac{1}{\sqrt{(L_1+L_2)C_1}}\sqrt{\frac{R_g^2 C_1}{4(L_1+L_2)} - 1}$$

3.2. Superconducting Materials SCM

This study presents a pioneering hybrid system that incorporates a Neodymium (NdFeB) permanent magnet as the limiting impedance, introducing a novel approach. The system is complemented by a specifically designed controller for operational regulation. The integration of the NdFeB permanent magnet as the limiting impedance brings several benefits, such as minimized size, cost, and weight, enhanced reliability, and the elimination of DC biasing and cooling costs [28, 29].

3.3. Model for a Hybrid HVDC Circuit Breaker

In HVDC systems, it is typical to represent each side of the system with an ideal DC voltage source linked in series with its corresponding impedance. This configuration allows for the modeling of HVDC transmission systems. Fig. 4 provides an illustration of a specific HVDC transmission system operating at 500 kV with a power capacity of 4400 MW. In this system, two MMCs are utilized to connect two high-voltage AC grids operating at 110 kV. MMC technology has gained significant popularity as the preferred voltage-source converter topology for HVDC applications. The use of MMCs offers several advantages, including better voltage control, enhanced power quality, reduced harmonics, and increased reliability. MMCs utilize multiple sub-modules, each consisting of several power semiconductor devices such as IGBTs or IGCTs. The sub-modules are arranged in a multilevel structure, allowing for improved waveform quality and voltage regulation in the HVDC system. By employing MMCs in HVDC systems, it becomes possible to efficiently transmit large amounts of power over long distances, interconnect different AC grids, and integrate renewable energy sources into the grid.

The simulation model, implemented in PLECS, considers the precise parameters of the ferromagnetic NdFeB materials, detailed in Table 1.

Table 1. Material properties of NdFeB [30]

Parameter	Symbol	Value
Winding turns	N	65
Core area (m^2)	A_{core}	0.04130
Length path (m)	L mean	1.5228
Remanence flux density (T)	T_{rem}	1.4
Saturation flux density (T)	T_{sat}	1.6
Coercivity (kA/m)	Hc	899.928
Coercivity of saturation (kA/m)	Hsat	1116.085
Resistivity (Ω m)	ρ	1.8 * 10−6
Free space permeability (H/m)	μ0	4π * 10−8

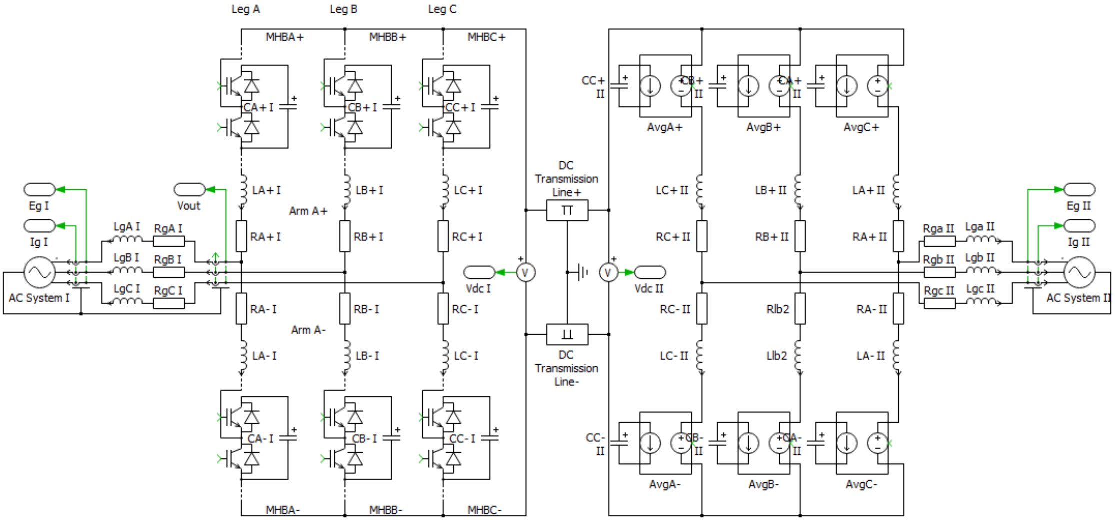


Fig. 4. Hybrid HVDC circuit breaker model using PLECS

MMCs contribute to the overall performance and stability of HVDC transmission systems, making them a popular choice in modern HVDC applications.

At high voltage levels, the transmission of direct current (DC) is known to be more efficient compared to alternating current (AC). The higher efficiency of high-voltage DC (HVDC) systems compared to high-voltage AC (HVAC) systems is a significant factor driving the increasing adoption of HVDC for power distribution purposes. This is particularly evident when integrating renewable energy sources located at a considerable distance from consumers, such as offshore wind farms. Consequently, there is a growing need for new types of converters that can effectively interface between different electricity networks, power sources, and loads.

MMC is a bidirectional voltage source converter used for connecting high-voltage AC and DC power systems. It consists of both positive and negative arms for each of the three phases. Each arm is composed of a series connection of switching submodules. The number of submodules is selected based on the desired harmonic performance and to enable the utilization of IGBTs. It is worth mentioning that this particular model is included as one of the demo models in the PLECS library. It also includes various model configurations accessible through the Configuration tab in the Simulation Parameter window, which can be found in the Simulation menu.

3.4. The simulation parameters for the proposed scheme

The simulation parameters used for the study are provided in Table 2, and the commutation circuit parameters were chosen to ensure the safety and effectiveness of the UFHFCL. It was noted that specific elements have a notable impact on the functionality of the UFHFCL, including the voltage source under fault conditions, discrimination current, pre-arcing time, and the duration for the recovery voltage to manifest across the mechanical contacts. These factors strongly influence the parameters of the commutation circuit. Through conducting simulations and scrutinizing the consequences of diverse parameters on the UFHFCL's performance, the proposed protection scheme's validity and efficacy can be appraised. It enables a better understanding of how the UFHFCL responds to fault conditions and assists in optimizing its performance in different scenarios.

4. Simulation Test of Proposed Scheme Using PLECS Program

4.1. Results of the Operation of UFHFCL

The design of the hybrid HVDC circuit breaker, as depicted in Fig. 1, can be effectively modeled, and simulated using different software packages, with Piecewise Linear Electrical Circuit Simulation Program (PLECS) tools being a particularly suitable option. Given the complexity of the circuit breaker design, which involves numerous semiconductor components, a modular approach can be adopted to represent different branches of the circuit breaker individually.

PLECS tools offer a modular representation advantage, allowing users to divide the hybrid HVDC circuit breaker model into separate modules, reflecting specific branches. This simplifies modeling, enhances simulation manageability, and accurately represents each branch's characteristics and behavior. The flexibility and ease of use of PLECS tools streamline the simulation process for the complex design, involving many semiconductor components. PLECS tools' user-friendly environment makes them well-suited for accurately representing the hybrid HVDC circuit breaker design. Overall, PLECS tools' modular representation capability, coupled with their simulation features, provide a reliable and efficient approach for accurately modeling and simulating the hybrid HVDC circuit breaker shown in Fig. 1. To substantiate the efficacy of the suggested UFHFCL, simulations were executed employing the PLECS software for the circuit illustrated in Fig. 1. During regular operational circumstances, the system sustains a 5-kA current, as illustrated in Fig. 5. Yet, in the event of a fault arising at 0.04 seconds, the potential fault current in the system elevates to 5 kA. This surge in fault current magnitude and voltage surpasses the power demands of devices functioning in the system, underscoring the imperative for UFHFCL deployment as a protective measure. The figure 5 shows the current of a load at normal and fault conditions. the current of the switch (I_{sw}). During normal operation, the current of the load is approximately 500 amperes, and the current of the switch is approximately 500 amperes. During a fault, the current of the load increases to approximately 5000 amperes and the time it takes for the switch current to reach its peak is approximately 0.005 seconds. Figure 6 show the voltage source at normal and fault mode. which is a much more erratic line that drops to around 3.5x10^5 V and then rebounds to around 4.5x10^5 V. The fault voltage is caused by a sudden increase in current, which lead to zero.

Table 2. Parameters of the UFHFCL for simulation

Parameter	**Value**
DC voltage Vdc	500 KV
Resistance Rs	0.02 mΩ
Inductance Ls	100e-3 H
Resistance of load R_{Load}	100.94 Ω
Inductance of load L_{Load}	200e-3 H
Inductance of commutation L_{Com}	200e-6 H
Capacitance of commutation C_{Com}	10e-6 F
Initial voltage of commutation capacitor V_{Com}	1200 V

Figure 7 presents a comparison between the theoretical analysis and simulation results of the interrupting methods, aiming to validate their accuracy and assess the effectiveness of the proposed method. Theoretical analysis provides a theoretical understanding of the interrupting process, while simulations allow for a more comprehensive evaluation by considering practical factors and system dynamics. The comparison in Fig. 7 demonstrates the agreement between the theoretical and simulation results, indicating the accuracy of the theoretical analysis and the reliability of the proposed interrupting method. The key parameters and performance metrics considered in the comparison include fault current interruption time, voltage waveform characteristics, current waveform characteristics, and other relevant factors. By comparing the theoretical and simulation results, it is possible to assess the agreement between the predicted performance of the interrupting method and its actual behavior in the simulated scenario. This comparison serves as a verification step to ensure that the theoretical analysis is reliable and that the proposed interrupting method functions as intended. The Fig. 7 provides a visual representation of the comparison, allowing for a direct evaluation of the agreement between the theoretical predictions and the simulation results. It helps to assess the effectiveness of the proposed method in interrupting the fault current and validates its performance under different fault conditions. This comparison between theoretical and simulation results contributes to the overall validation process of the proposed interrupting method and provides confidence in its accuracy and effectiveness in real-world applications.

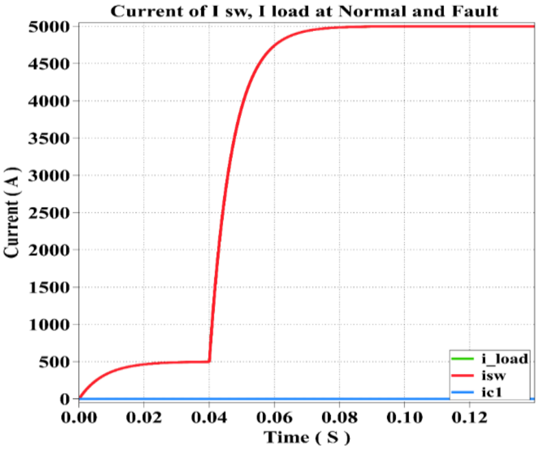


Fig. 5. Normal and prospective fault current

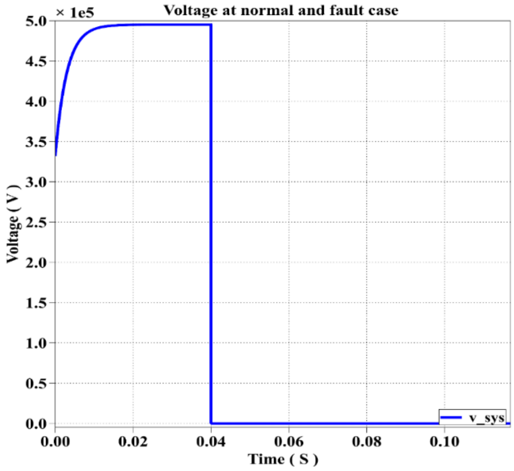


Fig. 6. Voltage source at normal and fault mode.

Figure.8 demonstrates the effectiveness of the UFHFCL in limiting the fault current during and after the insertion process. The operation of the FCLs successfully reduces the fault current from 5 KA to zero, which significantly decreases the demand for interrupting the fault current. Additionally, the UFHFCL causes the DC line current to decrease to zero at approximately 70.55 microseconds, which indicates the efficient performance of the UFHFCL in limiting the fault current magnitude. The small value of 70.55 microseconds indicates that the UFHFCL can rapidly and effectively limit the fault current, contributing to the protection and stability of the HVDC system. This observation further supports the claim that the UFHFCL is effective in controlling and mitigating fault currents, ensuring the safe operation of the system. The results shown in Fig. 9 provide evidence of the successful performance of the UFHFCL in limiting fault currents and highlight its significance in enhancing the overall reliability and stability of the HVDC system. The figure indicates the extent of the proposed system's response in limiting the fault current. Under normal conditions, the load current was 500 amps, and the capacitor current was zero. When a short circuit occurred for more than 0.04 seconds, the load current significantly increased to 3000 amps. Before reaching its maximum value, the capacitor current was injected and extinguished before reaching 2000 amps, with a very high time response rate.

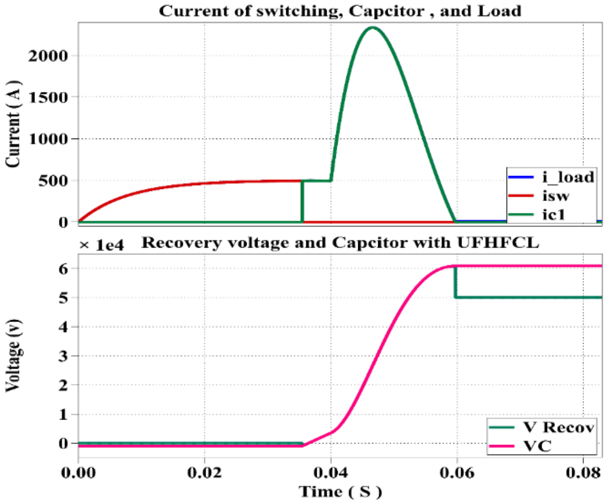


Fig. 7. Simulation results of fault currents .

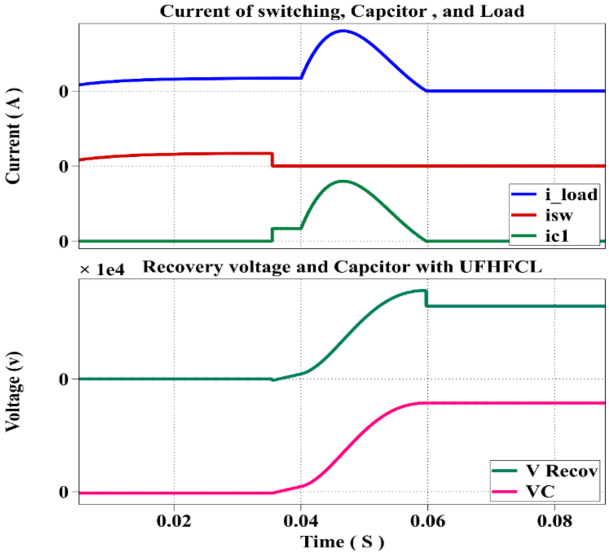


Fig. 8. Zoomed current and voltage waveforms of Fig.7.

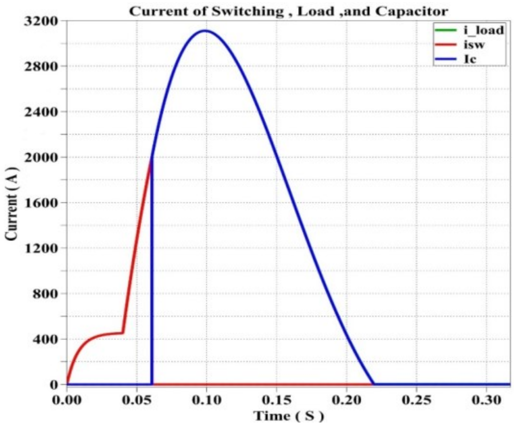


Fig. 9. UFHFCL performance in fault current limitation.

4.2. Effect of Fault Types on Hybrid DC FCL in HVDC System

In ultra-high voltage (UHV) transmission systems, DC faults can occur due to various reasons, such as insulation failure, lightning strikes, or equipment malfunction. These DC faults can result in high-magnitude fault currents, which can damage the transmission equipment, cause safety hazards, and even result in system shutdown. To mitigate these effects, FCL are often used in UHV transmission systems.

The occurrence of DC faults in UHV transmission systems can influence the effectiveness of FCLs. Two prevalent DC fault types in UHV systems are pole-to-pole faults and pole-to-ground faults. A pole-to-pole fault transpires when conductors from different poles of the HVDC system make contact, while a pole-to-ground fault arises when a conductor from one pole contacts the ground.

The impact of DC fault types on FCLs hinges on their design and operational features. Generally, FCLs can capably restrict fault current magnitudes in both pole-to-pole and pole-to-ground faults. However, pole-to-ground faults often result in higher fault current magnitudes compared to pole-to-pole faults. Consequently, FCLs may need to be designed to handle elevated fault currents in pole-to-ground fault scenarios.

The positioning of FCLs in UHV transmission systems is another factor influencing their efficacy. FCLs are typically strategically placed in the transmission system, such as near the converter station or at the midpoint of the transmission line. The optimal placement of FCLs can be determined based on anticipated fault current magnitudes and fault locations. The occurrence of DC faults in UHV transmission systems can impact FCL performance. Nevertheless, FCLs can proficiently limit fault current magnitudes in both pole-to-pole and pole-to-ground faults. Optimizing the design, operational characteristics, and placement of FCLs ensures their effective performance in UHV transmission systems.

4.3. Effect of Change of the Values of Both the Coil and the Capacitor in the UFHFCL

The values of both the coil and the capacitor in the DC FCL can affect the cut-off time and the recovery voltage values. Changing the values of the coil and the capacitor can alter the characteristics of the DC FCL, such as the inductance and capacitance of the device. As shown Fig. 10 and 11 Increasing the value of the coil in the DC FCL will increase the inductance of the device. The result in a longer cut-off time because the DC FCL will take longer to limit the fault current to a safe level. However, the recovery voltage will be reduced because the increased inductance will limit the rate of change of the current during the recovery period.

Conversely, increasing the value of the capacitor in the DC FCL will increase the capacitance of the device. This will result in a shorter cut-off time because the DC FCL will be able to limit the fault current more quickly. However, the recovery voltage will be increased because the increased capacitance will allow the voltage across the device to build up more quickly during the recovery period. Changing the values of both the coil and the capacitor in a hybrid DC FCL can affect the cut-off time and recovery voltage values of the device. Increasing the coil value will increase the cut-off time and decrease the recovery voltage, while increasing the capacitor value will decrease the cut-off time and increase the recovery voltage. It is important to choose the appropriate values of the coil and capacitor to ensure that the DC FCL performs optimally under different fault conditions.

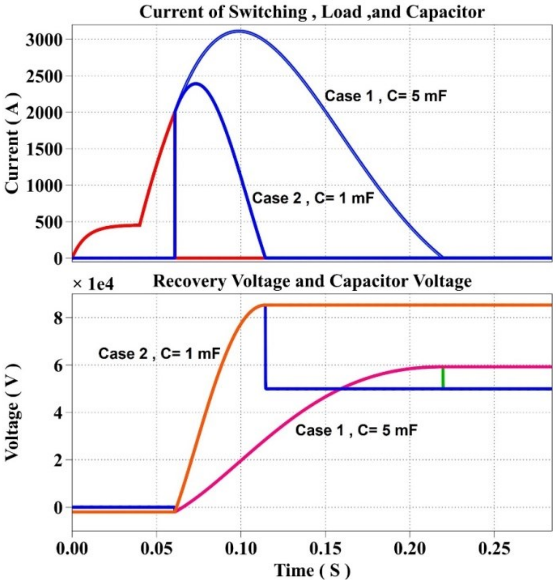


Fig. 10. current and voltage after increase the capacitor value in UFHFCL.

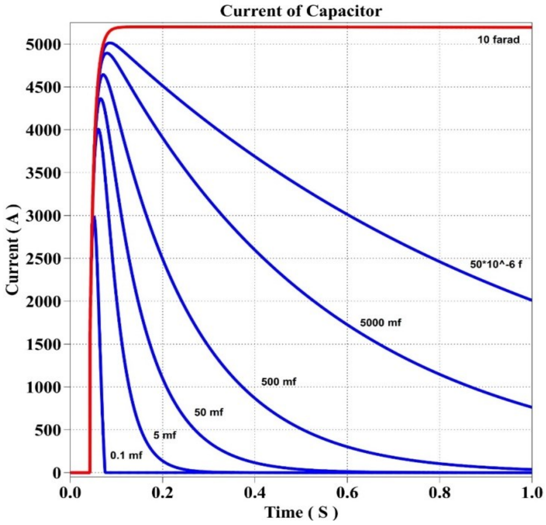


Fig. 11. current after increase the capacitor in different value in UFHFCL.

In a hybrid fault current limiter (HFCL) used in a DC system, the coil value refers to the inductance of the coil in the limiter circuit. The effect of changing the coil value can have several implications on the operation of the HFCL. Here are some potential effects:

Current limiting: The primary function of an HFCL is to limit fault currents during a short circuit or fault condition. By changing the coil value is adjust the level of fault current that the limiter can handle. Increasing the coil value typically leads to higher fault current limiting capabilities, while reducing the coil value may result in lower fault current limiting.as shown in Fig.12. Response Time: The response time of an HFCL refers to how quickly it can limit the fault current after a fault occurs. Altering the coil value can affect the response time of the limiter. Typically, increasing the coil value may result in a slower response time, while reducing the coil value can potentially improve the response time in Fig 13.

5. Experimental Setup

The experimental setup for the UFHFCL model encompasses crucial design considerations and incorporates a fault detection technique. The UFHFCL model is carefully designed to simulate real-world conditions, with a focus on the safe interruption of high-current DC faults. The setup incorporates key elements, including the main contact, semiconductor cells, and commutation components, to effectively control and interrupt fault currents. Additionally, the model features a fault detection technique that monitors and identifies fault conditions within the system promptly. This combination of hardware and fault detection methodology ensures that the UFHFCL can reliably and efficiently respond to DC faults, contributing to enhanced system safety and performance.

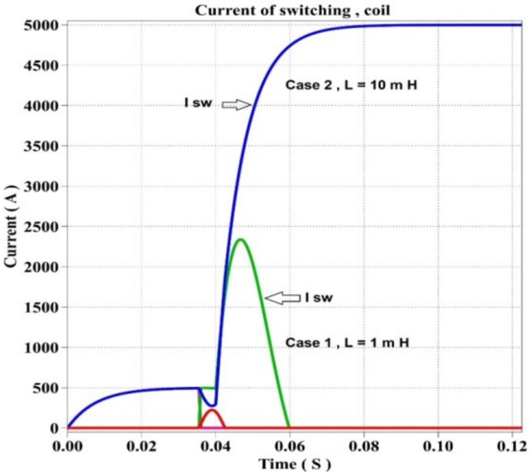


Fig. 12. current after changing the coil in different value in UFHFCL.

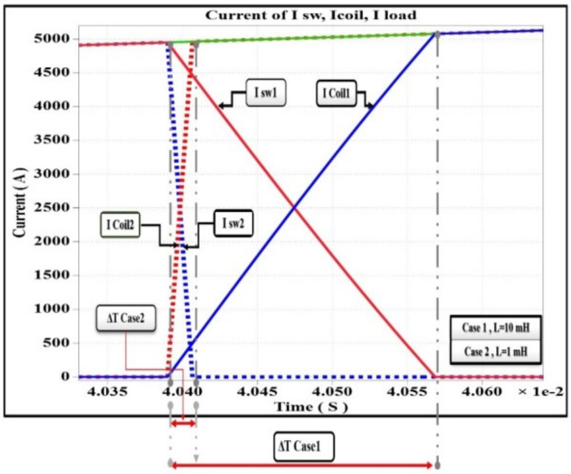


Fig. 13. currents after effect the coil in different value in UFHFCL.

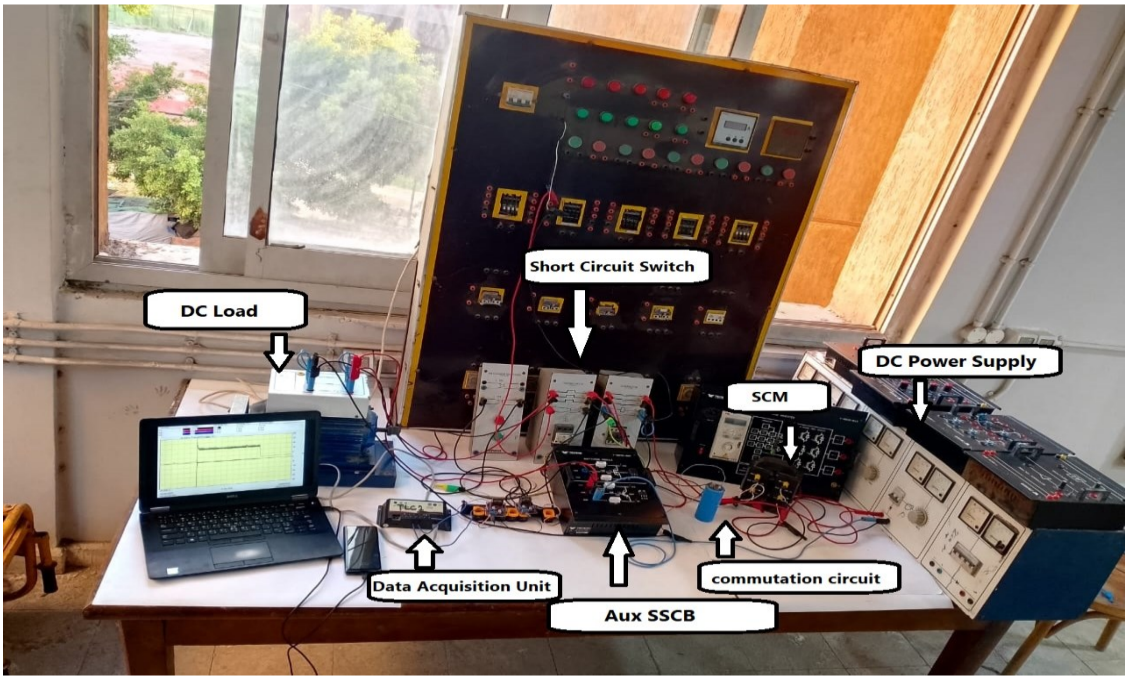


Fig. 14. Developed experimental prototype of UFHFCL.

The experimental arrangement incorporates measuring and protective instruments, as depicted in Fig. 14, for gauging and safeguarding various components. Moreover, the experimental circuit is linked to a Lab-top, enabling control, adjustment, and the printing of experiment output results.

In this section, a downscaled experimental prototype has been developed and executed to authenticate the simulation outcomes. The data about the prototype components can be found in Table 3. Fig. 14 illustrates the devised prototype arrangement. Upon fault detection, the UFHFCL is activated according to the operational flow chart provided in Fig.3.

The current and voltage waveforms, which illustrate the operational principles of the proposed technology, are portrayed in Figs. 15 and 16 under normal operating conditions and in the event of a fault, respectively. Notably, these figures do not include the integration of the UFHFCL into the system. Upon analysis of the data, the graph illustrates the behaviour of voltage and current in a circuit up to and during the occurrence of a fault at 0.027 seconds. Initially, both voltage and current follow typical patterns expected in a normal operating state. at a DC rated voltage of 220 V, it is observed that under normal conditions, the current stabilizes at 31 A. However, in the event of a fault, the current surges to 412.5 A when the fault occurs at the positive pole, as depicted in Fig. 15. Simultaneously, this value reaches to 754.2 A when a fault occurs at the negative pole, as illustrated in Fig. 16.

Figure 17, illustrates the efficacy of the proposed technology in managing fault currents through the utilization of superconducting materials. The figure shows the response of the proposed system to a short circuit, demonstrating its efficient handling of faults. The first curve displays the normal current levels, stabilizing at 33 amps. During a fault, the system accommodates a surge of up to 455 amps, an increase of approximately 14 times, indicating a significant tolerance to high fault currents. As the fault is rectified, the current gradually decreases and stabilizes at 63 amps, indicating successful restoration of normal circuit operation. The diagram also highlights the system's rapid response time to fault currents, reaching its peak in just 0.005 seconds. This quick reaction time allows the system to promptly detect and mitigate faults, minimizing potential damage or hazards. The system's ability to handle fault currents swiftly enhances reliability and safety by protecting against sudden disruptions. The depicted results demonstrate the technology's success to reduce the current to about 85% of initial fault current, (i.e. limited to less than three times the expected fault current).

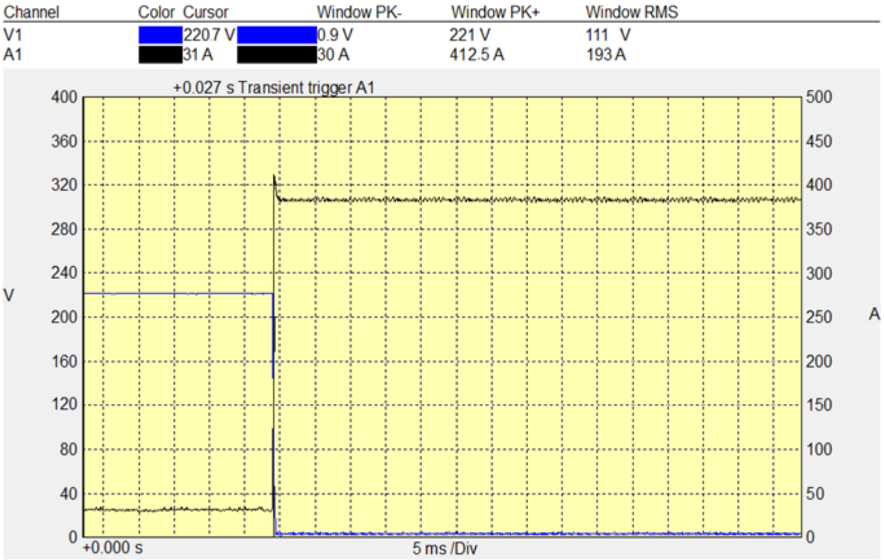
During laboratory tests, UFHFCL succeeded in limiting and interrupting the fault current, when the fault current is successfully interrupted and reaches zero, a transient recovery voltage (TRV) appears on a fast-mechanical switch. Leveraging SFCL technology proves instrumental in swiftly reducing the transient recovery voltage to levels close to the rated voltage as shown in Figs. 18 and 19 This enhancement ensures efficient and controlled electrical system operation following fault current interruption.

The experimental findings underscore the effectiveness of the proposed UFHFCL approach in accurately identifying and managing fault currents within HVDC systems. By leveraging the superconducting element, the UFHFCL demonstrates the capability to efficiently constrain and interrupt fault currents. This not only ensures the prompt isolation of faulted sections but also aids in delaying the onset of the recovery voltage on the mechanical disconnect switch.

Specifically, the UFHFCL exhibits a remarkable ability to swiftly reduce the recovery voltage to levels well within the safe operational limits of the HVDC system. In practical terms, this means that the UFHFCL can mitigate the risk of overvoltage's by promptly limiting the fault currents and subsequently managing the recovery process. This aspect is crucial for maintaining the stability and integrity of the HVDC grid, especially during fault conditions. Moreover, the experimental results indicate that the UFHFCL contributes to enhancing the overall reliability and performance of HVDC systems. By effectively curtailing fault currents and managing recovery voltages, the UFHFCL plays a pivotal role in minimizing downtime and mitigating potential damage to equipment. This translates to significant improvements in system uptime and operational efficiency, ultimately benefiting both utilities and end-users. Overall, the experimental findings provide compelling evidence of the practical efficacy and feasibility of implementing UFHFCL technology in real-world HVDC systems. The demonstrated ability to accurately identify fault currents, constrain over voltages, and enhance system reliability underscores the potential of UFHFCL as a key component in modern HVDC grid protection strategies.

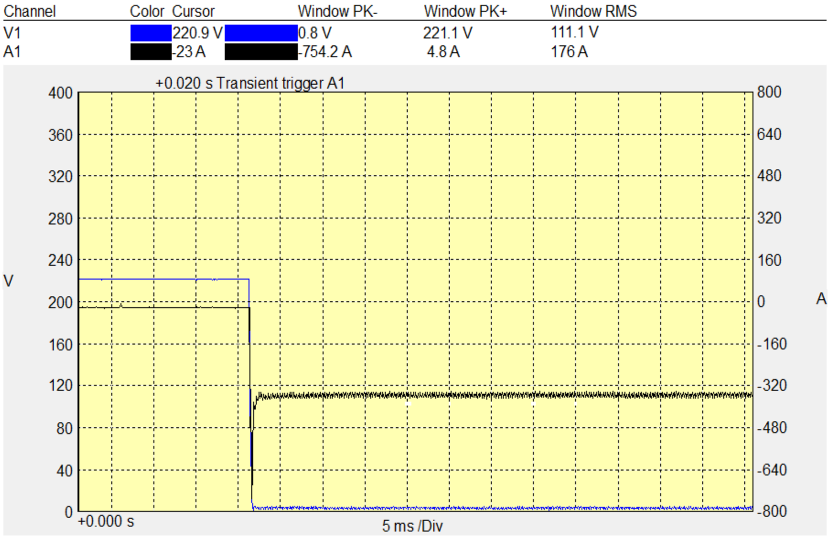
Table 3. Experimental setup parameters

Symbol	Description	Value
V_{dc}	Nominal voltage	220 V
I_{Load}	Load current	31 A
R_{Line}	Line resistance	0.5 Ω
L_{Line}	Line inductance	30 mH
R_d	DC reactor resistance	0.1 Ω
L_d	DC reactor inductance	100 mH
C	DC link capacitor	100 mF
R1	MB series resistor (Magnetic Breaker 1)	2 Ω
R2	MB series resistor (Magnetic Breaker 2)	2 Ω
R3	DC reactor damping resistor	200 Ω
RF	Resistance of the fault	0.01 Ω
LCS	IGBT	500 V, 10 A
MB	IGBT	1000 V, 20 A



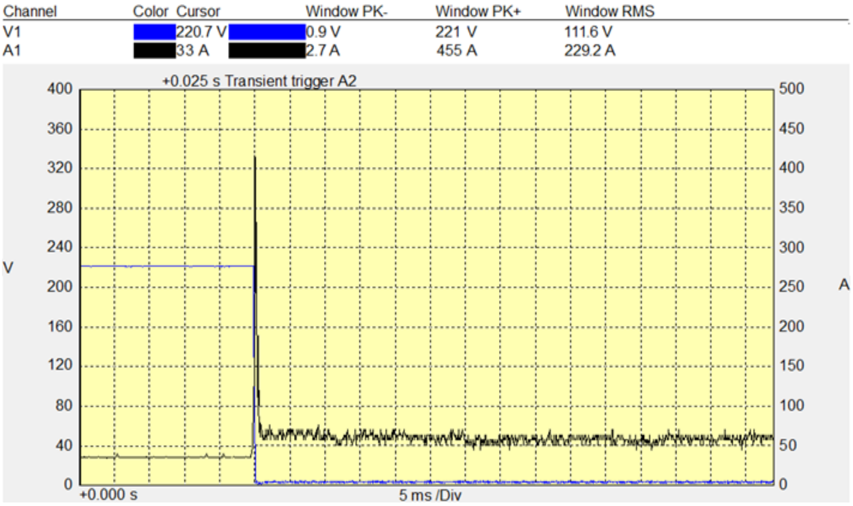
Channel	Color Cursor	Window PK-	Window PK+	Window RMS
V1	🟦 220.7 V	🟦 0.9 V	221 V	111 V
A1	⬛ 31 A	⬛ 30 A	412.5 A	193 A

Fig. 15. The current and voltage waveforms during normal operation and fault condition.



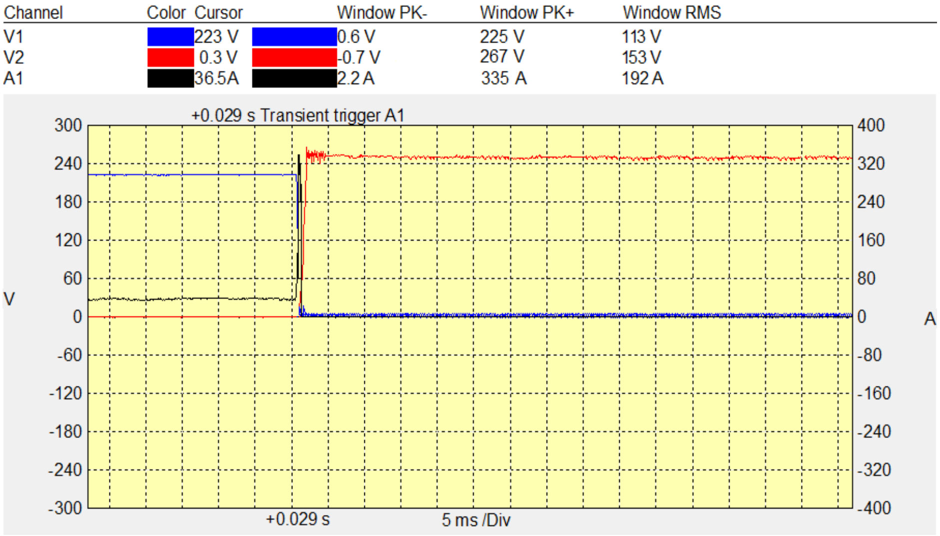
Channel	Color Cursor	Window PK-	Window PK+	Window RMS
V1	🟦 220.9 V	🟦 0.8 V	221.1 V	111.1 V
A1	⬛ -23 A	⬛ -754.2 A	4.8 A	176 A

Fig. 16. The response of the system after insert the SFCL to the system.



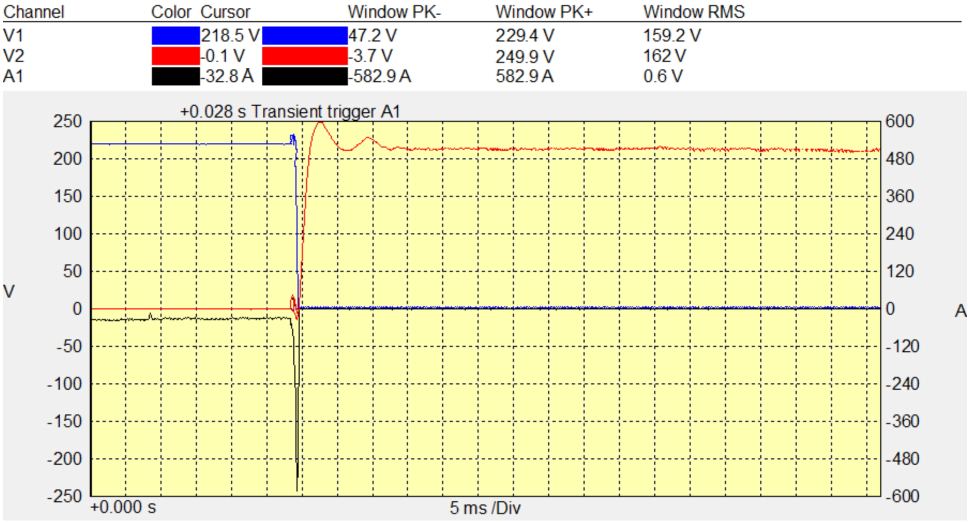
Channel	Color Cursor	Window PK-	Window PK+	Window RMS
V1	🟦 220.7 V	🟦 0.9 V	221 V	111.6 V
A1	⬛ 33 A	⬛ 2.7 A	455 A	229.2 A

Fig.17. The system response to limit 85% of the initial fault current without interruption.



Channel	Color	Cursor		Window PK-	Window PK+	Window RMS
V1	🟦	223 V	🟦	0.6 V	225 V	113 V
V2	🟥	0.3 V	🟥	-0.7 V	267 V	153 V
A1	⬛	36.5A	⬛	2.2 A	335 A	192 A

Fig. 18. The response of UFHFCL to limit and interrupt the fault current during positive pole current.



Channel	Color	Cursor		Window PK-	Window PK+	Window RMS
V1	🟦	218.5 V	🟦	47.2 V	229.4 V	159.2 V
V2	🟥	-0.1 V	🟥	-3.7 V	249.9 V	162 V
A1	⬛	-32.8 A	⬛	-582.9 A	582.9 A	0.6 V

Fig. 19. The response of UFHFCL to limit and interrupt the fault current during negative pole current.

Table 4. Cost comparison table between UFHFCL and other systems [31-33]

Aspect	**UFHFCL**	**SSCB**	**MCB**
Initial Equipment Cost	Higher	Moderate	Lower
Installation Cost	Moderate	Moderate	Lower
Maintenance Cost	Moderate	Lower	Higher
Operating Cost	Lower (Energy Efficient)	Moderate	Lower
Lifespan	Longer	Moderate	Shorter
Downtime and Repair Cost	Lower (Solid-State Technology)	Lower (Fewer Moving Parts)	Higher (Mechanical Wear)

5.1. Limitations and Potential Challenges of Implementing The UFHFCL in Practical HVDC Systems

After implementing the UFHFCL technology in my research, several limitations, and potential challenges in practical HVDC systems became apparent. These challenges include:

- Implementing UFHFCL technology involves significant upfront costs, including the development and installation of high-frequency transformers and superconducting materials. The economic feasibility of large-scale deployment needs careful consideration.
- Superconducting materials, while offering unique benefits, can be sensitive to external factors such as temperature and magnetic fields. Ensuring the long-term reliability and stability of these materials poses a challenge that requires ongoing maintenance and monitoring.
- The scalability of UFHFCL for high-power HVDC systems must be carefully considered. Ensuring the technology's effectiveness and reliability at elevated power levels without compromising other system parameters is a significant challenge.
- The integration of UFHFCL into existing HVDC systems may be complex and require modifications to the infrastructure. Compatibility issues with different HVDC configurations and the need for synchronized operation with other protection devices must be addressed.

5.2. Comprehensive Cost Comparison Table between UFHFCL and Other Systems

A comparison table between UFHFCL and other systems in terms of cost can be helpful for evaluating their economic feasibility.

While providing an exact comparison might be challenging due to the diverse range of existing systems and their specific configurations, we can offer some insights based on our analysis and industry standards in the following table:

The UFHFCL system presents several advantages, including enhanced safety and technical efficiency. However, it's essential to acknowledge that the cost of implementing such a system can vary depending on factors such as the scale of the application, geographical location, and specific requirements of the power infrastructure.

Generally, the UFHFCL system may involve higher initial investment costs compared to conventional solutions. However, these costs could potentially be offset by long-term benefits, such as reduced downtime, enhanced reliability, and improved system stability, resulting in overall cost-effectiveness over the system's lifecycle.

5 Conclusion

In conclusion, the integration of UFHFCLs in HVDC systems offers a multitude of advantages, marking a significant leap in the realm of HVDC protection. The experimental and theoretical findings collectively underscore the transformative impact of UFHFCLs on HVDC system performance. The UFHFCLs exhibit a range of compelling benefits, including high-speed protection mechanisms, bolstered power system stability, heightened reliability, compact physical footprint, minimal power loss, robust fault-handling capabilities, and an economically feasible design. The experimental results meticulously align with the anticipated theoretical outcomes, illustrating the remarkable ability of UFHFCLs to swiftly limit fault currents within microseconds. This rapid response not only prevents harm to other critical system components but also mitigates the potential for cascading failures that could jeopardize the entire HVDC system.

The versatility displayed by UFHFCLs in effectively managing various types of DC faults positions them as a holistic and comprehensive solution for HVDC system protection. The practical results derived from experimental tests serve as a robust affirmation, establishing UFHFCLs as a reliable and highly effective means of safeguarding HVDC systems. Through their deployment, UFHFCLs significantly contribute to enhancing the safety, stability, and overall performance of HVDC systems, marking a noteworthy advancement in the field of electrical power systems protection.

Appendix A

Abbreviation	Definition
HVDC	High Voltage Direct Current
FCL	Fault Current Limiter
HDCCB	Hybrid Direct Current Circuit Breaker
SCM	Superconductor Material
UFHFCL	Ultra-Fast Hybrid Fault Current Limiter
PLECS	Piecewise Linear Electrical Circuit Simulation
MCB	Mechanical Circuit Breaker
SSB	Solid State Breaker
UHV	Ultra-high voltage
SFCL	Superconducting fault current limiter
CLR	Capacitor coil resistance path
MCB	mechanical circuit breaker
IGBT	insulated-gate bipolar transistors
UFD	ultrafast disconnector
MOV	Metal Oxide Varistors
ZnO	Zinc Oxide varistors
IGCT	integrated gate-commutated thyristor
MMC	modular multi-level converters
MRI	magnetic resonance imaging
HTS	high-temperature superconductors
NdFeB	Neodymium permanent magnet
DBN	deep belief network

Acknowledgements

The authors would like to express their sincere appreciation to Suez University and the Technological Colleges in Alexandria for their valuable support in enriching this article and facilitating its practical implementation.

Author Contributions

S. A. M. A., H. E. M. A, S. H., I. S, A.M. H. was responsible for the conceptualization, validation, resources, data curation, software development. S. A. M. A., H. E. M. A, S. H., I. S, A.M. H. jointly contributed to the methodology, formal analysis, investigation, original draft preparation, review and editing, visualization, supervision. All authors have read and agreed to the published version of the manuscript.

Conflict of Interest

The author(s) declared no potential conflicts of interest with respect to the research, authorship, and publication of this article.

References

[1] S. Xu, Q. Song, Y. Zhou, J. Meng, W. Yang, B. Zhao, and R. Zeng, "Dynamic model of the DC fault clearing process of a hybrid modular multilevel converter considering commutations of the fault current," IEEE Transactions on Power Electronics, vol. 35, no. 7, pp. 6668–6672, 2019.

[2] Y. A. Amor, G. Didier, J. Leveque, and F. Hamoudi, "Study on the alliance between SFCL and hybrid DC circuit breaker for protecting HVDC grid," Journal of Physics: Conference Series, vol. 1559, no. 1, p. 012102, 2020.

[3] O. Cwikowski, M. Barnes, R. Shuttleworth, and B. Chang, "Analysis and simulation of the proactive hybrid circuit breaker," in Proc. 2015 IEEE 11th Int. Conf. on Power Electronics and Drive Systems (PEDS), 2015, pp. 4–11.

[4] J. Shi, Y. Tang, L. Chen, J. Wang, L. Ren, J. Li, and L. Li, "The application of active superconducting DC fault current limiter in hybrid AC/DC power supply systems," IEEE Transactions on Applied Superconductivity, vol. 18, no. 2, pp. 672–675, 2008.

[5] A.J. Far and D. Jovcic, "Design, modeling and control of hybrid DC circuit breaker based on fast thyristors," IEEE Transactions on Power Delivery, vol. 33, no. 2, pp. 919–927, 2017.

[6] C. Ding, T. Nie, and Y. Chen, "A distribution network solid-state DC circuit breaker with current limiting function," Energy Reports, vol. 8, pp. 986–994, 2022.

[7] A. Ghaemi, A. Safari, H. Afsharirad, and H. Shayeghi, "Accuracy enhancement of fault classification and location in a smart distribution network based on stacked ensemble learning," Electric Power Systems Research, vol. 205, p. 107766, 2022.

[8] J. Liu, N. Tai, C. Fan, and S. Chen, "A hybrid current-limiting circuit for DC line fault in multiterminal VSC-HVDC system," IEEE Transactions on Industrial Electronics, vol. 64, no. 7, pp. 5595–5607, 2017.

[9] R. Lazzari and L. Piegari, "Design and implementation of LVDC hybrid circuit breaker," IEEE Transactions on Power Electronics, vol. 34, no. 8, pp. 7369–7380, 2018.

[10] X. Zhang, C. Zhuo, and X. Yang, "A natural commutation current topology of hybrid HVDC circuit breaker integrated with limiting fault current," IET Generation, Transmission & Distribution, vol. 17, no. 7, pp. 1509–1524, 2023.

[11] S.Y. Park and H.S. Choi, "Operation characteristics of superconducting DC circuit breaker for reliability assessment in a transient state of MMC VSC-HVDC," Journal of Electrical Engineering & Technology, pp. 1–9, 2023.

[12] A.M.H., M. Shivakumar, and R.S. Aradhya, "Solid state fault current limiter (SSFCL) in power system – a case study," in Proc. Int. Conf. on Sustainable Engineering and Technology (iConSET), 2018.

[13] S. Liang, Y. Tang, L. Ren, Y. Xu, Z. Xia, Z. Wang, and S. Guo, "Tests and analysis of a small-scale hybrid-type DC SFCL prototype," IEEE Transactions on Applied Superconductivity, vol. 28, no. 4, pp. 1–6, 2018.

[14] S. A. M. Abdelwahab, A. M. Hamada, H. Attia, I. Shoaaib, and S. Hasan, "A novel non-superconducting fault current limiter for enhancing the reliability and stability of electrical distribution grids," Industrial Technology Journal, 2024, doi: 10.21608/itj.2024.266234.1010.

[15] M. Steurer, K. Frohlich, W. Holaus, and K. Kaltenegger, "A novel hybrid current-limiting circuit breaker for medium voltage: Principle and test results," IEEE Transactions on Power Delivery, vol. 18, no. 2, pp. 460–467, 2003.

[16] S. Tang, M. Chen, G. Jia, and C. Zhang, "Topology of current-limiting and energy-transferring DC circuit breaker for DC distribution networks," CSEE Journal of Power and Energy Systems, vol. 6, no. 2, pp. 298–306, 2020.

[17] N. Belda and R. Smeets, "Test circuits for HVDC circuit breakers," IEEE Transactions on Power Delivery, vol. 32, no. 1, pp. 285–293, 2016.

[18] M. Bonkarev, N.K. Challagondla, and D. Thummapal, "Simulation-based performance evaluation of different current breaking techniques employed in mechanical HVDC circuit breakers," in Proc. IEEE Int. Conf. on High Voltage Engineering and Application (ICHVE), 2016, pp. 1–4.

[19] B. Xiang, L. Gao, Z. Liu, Y. Geng, and J. Wang, "Short-circuit fault current-limiting characteristics of a resistive-type superconducting fault current limiter in DC grids," Superconductor Science and Technology, vol. 33, no. 2, p. 024005, 2020.

[20] L. Chen, H. Chen, Z. Shu, G. Zhang, T. Xia, and L. Ren, "Comparison of inductive and resistive SFCL to robustness improvement of a VSC-HVDC system with

wind plants against DC fault," IEEE Transactions on Applied Superconductivity, vol. 26, no. 7, pp. 1–8, 2016.

[21] A. Maistrello, E. Gaio, A. Ferro, M. Perna, C. Panizza, F. Soso, and L. Novello, "Experimental qualification of the hybrid circuit breaker developed for JT-60SA quench protection circuit," IEEE Transactions on Applied Superconductivity, vol. 24, no. 3, pp. 1–5, 2013.

[22] F. Zhang, Y. Ren, Z. Shi, X. Yang, and W. Chen, "Novel hybrid DC circuit breaker based on series connection of thyristors and IGBT half-bridge submodules," IEEE Transactions on Power Electronics, vol. 36, no. 2, pp. 1506–1518, 2020.

[23] Z. Yu, Z. Gan, L. Qu, X. Yan, X. Wang, and Y. Huang, "Natural commutation type hybrid DC circuit breaker based on hybrid mechanical gaps," IEEE Transactions on Power Delivery, 2022.

[24] L. Feng, R. Gou, X. Yang, F. Wang, F. Zhuo, and S. Shi, "A 320 kV hybrid HVDC circuit breaker based on thyristors forced current zero technique," in Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC), 2017, pp. 384–390.

[25] H. Nakao, Y. Nakagoshi, M. Hatano, T. Koshizuka, S. Nishiwaki, A. Kobayashi, and T. Murao, "DC current interruption in HVDC SF6 gas MRTB by means of self-excitation," IEEE Power Engineering Review, vol. 21, no. 8, p. 62, 2001.

[26] T. Wei, Z. Yu, Z. Chen, X. Zhang, W. Wen, Y. Huang, and R. Zeng, "Design and test of the bidirectional solid-state switch for a 160 kV/9 kA hybrid DC circuit breaker," in Proc. IEEE Applied Power Electronics Conf. and Exposition (APEC), 2018, pp. 141–148.

[27] Z. Chen, Z. Yu, X. Zhang, T. Wei, G. Lyu, L. Qu, and Y. Huang, "Analysis and experiments for IGBT, IEGT, and IGCT in hybrid DC circuit breaker," IEEE Transactions on Industrial Electronics, vol. 65, no. 4, pp. 2883–2892, 2017.

[28] A.M. Hamada, A.R. Ahmed, and S. Hassan, "A comprehensive review on superconducting and non-superconducting FCLs for power network," International Journal of Advances in Engineering and Management, vol. 4, pp. 1003–1017, 2022.

[29] S. Hasan, E.S. El-Refaie, A.H.K. Alaboudy, and A. Hamada, "An AC hybrid current limiting and interrupting device for low voltage systems," Alexandria Engineering Journal, vol. 57, no. 3, pp. 1535–1548, 2018.

[30] J.R. Prigmore, J. A. Mendoza, and G. G. Karady, "Comparison of four different types of ferromagnetic materials for fault current limiter applications," IEEE Transactions on Power Delivery, vol. 28, no. 3, pp. 1491–1498, 2013.

[31] A.M. Hamada, S.S.M. Ghoneim, S.A.M. Abdelwahab, and W. S. E. Abdellatif, "Performance analysis of three-phase hybrid fault current limiter with one commutation circuit," International Journal of Electrical Power & Energy Systems, vol. 133, 2021.

[32] S.A.M. Abdelwahab, A.M. Hamada, S. Hasan, R. Salem, and W. S. E. Abdellatif, "Design and experimental investigation of three-phase inductive type superconducting fault current limiter based on current injection method," International Journal of Renewable Energy Research (IJRER), vol. 13, no. 3, 2023.

[33] A.M. Hamada, W.S.E. Abdellatif, S. A. M. Abdelwahab, and M. M. R. Ahmed, "Development of an arcless hybrid DC fault current limiter suitable for DC railway power networks," International Journal of Electrical Power & Energy Systems, vol. 157, 2024, doi: 10.1016/j.ijepes.2024.109822.