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A Novel Switched Capacitor Boosting Nine-level Inverter for Solar applications

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Abstract- The evaluation of Switched-Capacitor-Based Multilevel Inverters (SCMLIs) involves the use of a 'cost function' (CF) that incorporates key parameters such as devices count, total standing voltage (TSV), and source requirements. In this study, a nine-level inverter is designed with the goal of achieving a minimal CF value and a reduced switch count while enhancing its boosting capabilities. To accomplish voltage boosting of four, the suggested SCMLI employs two capacitors and single DC source. It necessitates eleven switches, four of them having a peak inverse voltage (PIV) limited to source voltage. The rest of seven switching devices have PIV limited to double the source voltage. As a result, all operating switches have PIV less than the peak amplitude of output voltage. The proposed topology is investigated using level-shifted pulse width modulation strategy. The performance of configuration that is proposed is initially analysed through MATLAB/Simulink simulations, accommodating diverse parameter modifications. Additionally, it incorporates switched capacitor design and estimation of power losses in devices. Thermal modelling utilizing PLECS is employed to assess power losses and efficiency. A thorough comparative analysis of existing topologies is undertaken to illustrate the superior performance of the suggested structure in addressing essential aspects. Then, hardware-in-loop (HIL) experiments are conducted to validate the practicality of the research and the functionality of the proposed topology.

Keywords Multi-level inverter (MLI), total standing voltage (TSV), switched capacitor (SC), reduced switch count, OPAL-RT(OP4510), level shifted pulse width modulation (LSPWM).

1. Introduction

Multilevel inverters (MLIs) are gaining popularity across various applications due to their attractive advantages, including reduced dv/dt, improved waveform quality, and minimized power losses [1-2]. When operating with voltage levels exceeding three, the commonly used MLIs include Cascaded H-bridge, Neutral-Point Clamped and Flying Capacitor configurations. Recently, significant efforts are made to minimize switches count, address challenges related to capacitor voltage balancing, eliminate the need for additional DC sources, and refine control strategies [3-5]. As a result, MLIs can currently be categorized into two groups: those utilizing a single DC source with boosting capability and those employing multiple DC sources without boosting capabilities. Boosting-based switched capacitor topologies are highly favored compared to other categories [6-7]. Cascaded configuration topologies operate either in a symmetrical or asymmetrical mode, depending on the proportion of isolated sources [8-9]. In SC-based configurations involving huge number of switches, capacitors are in series to create voltage

levels [10-11]. [12] presents a step-up configuration with a minimal switch count and balanced capacitor voltages.

The SC-based Multilevel Inverter (MLI) offers numerous advantages that make it suitable for renewable energy as well as solar PV rooftop applications [13]. A modified T-type inverter is often employed for medium-power applications [14]. [15] introduces a novel boosting capability for a switched capacitor (SC)-based inverter using a Marx structure. By integrating Marx structure units with the existing H-bridge, the inverter can achieve higher levels [16]. In [17], a cascaded Multilevel Inverter (MLI) was constructed using front and back-end entities, connected to two isolated sources. The front-end device in this configuration is the switched capacitor, while the back-end is comprised of the H-bridge.

[18] describes a hybrid switched capacitor MLI that employs an isolated source, a single capacitor and complementary devices linked in series/parallel mode. Combining the basic structure in series allows for the attainment of higher voltage levels. Consequently, the SC-MLI designs outlined [19-20] exhibit inherent balanced capacitor voltages and performance enhancements, making them highly suitable for alternative energy conversion. While both designs offer the same output voltage levels and device counts, [19] utilizes one additional capacitor compared to [20] to achieve superior voltage boosting capabilities. Additionally, [21] implemented the SC technique to suggest an extended voltage boost MLI.

To acquire desired levels, semiconductor devices and capacitors are interconnected in series or parallel with the power source. Employing six switches and two capacitors in cross connected design, and the output voltage level is determined by count of cross connected sections [21]. In [22], two topologies are proposed that utilize a pair of power sources and capacitors.[23] presents a switched capacitor-based hybrid design for a nine-level inverter. However, these topologies while providing nine-levels, lack the inherent boosting feature. In [24], voltage enhancement is achieved by integrating a non-isolated buck-boost converter and inverter that uses two capacitors.[25] Switched Capacitor (SC) technique is employed to generate a quasi-resonant design. To achieve the required output voltage levels, a choke coil is incorporated into the circuit.

Repetitive SC groups are interconnected at opposite ends of two T-type structures [26]. A nine-level inverter is combined with a series/parallel arrangement of capacitors (H9ISPC) [27]. By balanced voltage of capacitors, this configuration increases voltage levels while maintaining a constant voltage output. An Active Neutral Point Clamped (ANPC) inverter structure with a gain of 1 is presented [28].[29] describes a five-level inverter that utilizes the switched capacitor approach with four switches and a single capacitor. The output voltage level is increased by cascading multiple modules. A novel T-type inverter with triple boost capability is proposed [30]. The configuration comprises a series/parallel arrangement of capacitors, with an inductor in series to source. The total number of capacitor sections cascaded with the previous modules determines the output voltage level.

An analysis of H-bridge-based inverter is presented [31], implemented for three-phase utility applications. This design maintains balanced voltages across capacitors but lacks the capability for voltage boosting.[32] introduces the CGT boost inverter, where the boost converter is used as the main Multilevel Inverter (MLI) by connecting switches and capacitors in series/parallel configurations. A triple boost diamond-shaped architecture considering minimal Total Standing Voltage (TSV) in [33].

In [34], the authors introduced a layout with a minimal number of components, highlighting its regenerative capability. This means that if the capacitors become overcharged, they can release capacitive energy back to the source. In [35,41] a generalized configuration is developed by connecting a larger proportion of Switched Capacitor (SC) networks, each consisting of a pair of semiconductor devices, one diode, and one capacitor.[36] introduces a system where voltage levels are generated through two units: one is a generating unit that contains semiconductor devices and capacitors, and other is an H-bridge unit. A nine-level switched capacitor (SC) inverter in [37], utilizing both unipolar and bipolar semiconductor devices along with two capacitors.

[38] presents a seven-level switched capacitor topology with triple boosting capability, enabling it to achieve a minimum of three gains to generate suitable grid voltages, particularly for low-voltage photovoltaic (PV) panels. In [39], four semiconductor devices are employed to handle peak output voltage. A thirteen-level structure utilizing thirteen devices and three capacitors is outlined [40]. DC-DC converter configurations related to PV applications are discussed in [42,43]. Modelling analysis of three phase inverter for solar appliances is presented in [44]. Comparison between well-established MLIs with packed U-Cell inverters are described in [45]. Design methodology of novel resonant inverter is presented [46]. It is important to note that designs with a higher proportion of high peak voltage stress on devices lead to a high Total Voltage Stress (TVS) for the configuration. It is clear from this discussion that the main challenges of the suggested nine-level SC inverters are their substantial component demands, higher voltage stress, low efficiency, and minimal cost factor.

The key objective is to develop a novel single-phase system design utilizing switched capacitor approach which permits the current path conduction to incorporate minimal count of power devices. In this article, a quadruple boost, nine-level (9L) inverter is proposed for applications involving low voltage such as solar panels, electric vehicles (EVs), and other high-power quality requirements. Figure 1 illustrates the connection of rooftop solar panels, a DC-DC converter, and various loads through the proposed Switched Capacitor Multilevel Inverter (SC MLI).

The primary contributions of this work are outlined as follows:

- Introducing a novel SCMLI topology with a reduced switch count, enhancing both technical and economic benefits over the traditional H-bridge inverter. This

innovative design stands as a significant achievement of the present work.

- Developing an analytical mathematical model that optimally utilizes capacitors to achieve the desired voltage level at the load end. This model ensures efficient utilization of resources, contributing to the overall effectiveness of the proposed system.
- Conducting extensive experiments on an interconnected system and validating the results using a real-time simulator. The obtained outcomes are meticulously compared with those from recent approaches, providing valuable insights into the performance and superiority of the proposed methodology.

In summary, the outlined configuration adeptly tackles various critical factors, including boosting capability, simplicity, device stress, self-balancing, efficiency, and cost-effectiveness. Furthermore, the structure of this work is outlined as follows: Section II presents an overview of the proposed topology's operation, elucidating its functionality and detailing the various modes of operation. It also provides a brief description of the employed control method. In Section III, the paper delves into technical aspects such as voltage stress on components, current ratings of switches and diodes, calculations related to capacitors, and a comprehensive loss computation. These analyses are performed to assess the efficiency and effectiveness of suggested design. Section IV focuses on simulation results, including thermal modelling using PLECS software, hardware-in-loop (HIL) outcomes, offering practical insights into the system's performance and conducts a comparative analysis, contrasting the suggested configuration with recent research, emphasizing its distinctive features and advantages. Finally, Section V presents the conclusion, summarizing the key findings and contributions related to the proposed Multilevel Inverter (MLI) topology and its applications.

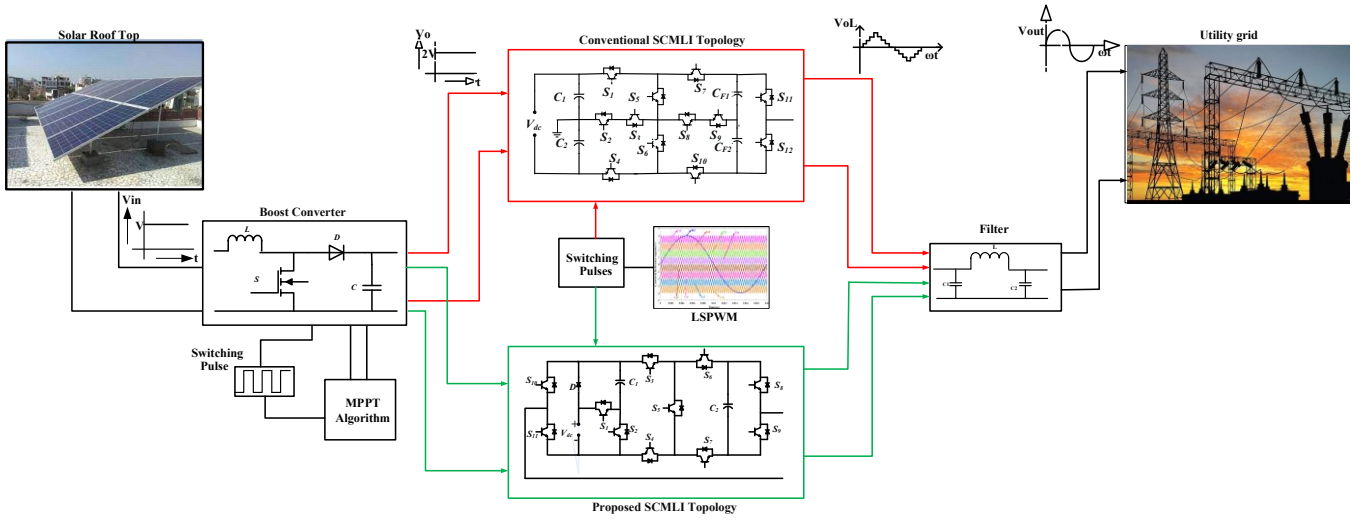


Fig. 1. Interconnection of MLI with solar panel.

2. Proposed Topology

2.1. Circuit Configuration

Figure 2 illustrates the proposed configuration consisting of eleven switches (parallel IGBT with diode), one diode, two capacitors, and an isolated DC source. Table 1 and figure 2 provide details about the topology's modes of operation and indicate the direction of current for each output level. In Table 1, the value "1" indicates that a specific switch is ON, whereas "0" signifies that it is OFF. Each switching mode listed in Table I has a unique impact on the voltages across capacitors. By employing these switching modes, a balanced distribution of voltages (V_{dc} and $2V_{dc}$) is achieved across capacitors C_1 and C_2 respectively.

2.2. Operating Modes

Figure 3 illustrates all the operational modes from A to I. Each mode is represented with two colours based on the required directions: (a) the path indicating the level of generation is represented as green, and (b) the path utilized for capacitor charging is represented in purple.

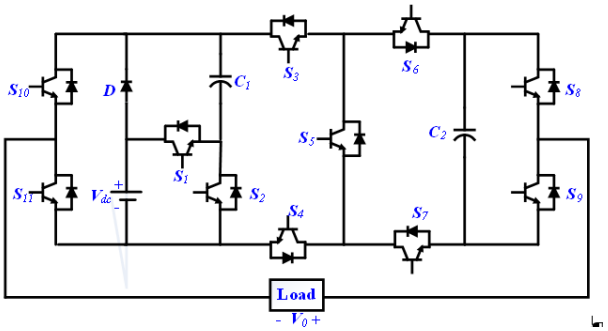


Fig. 2. Proposed nine-level topology.

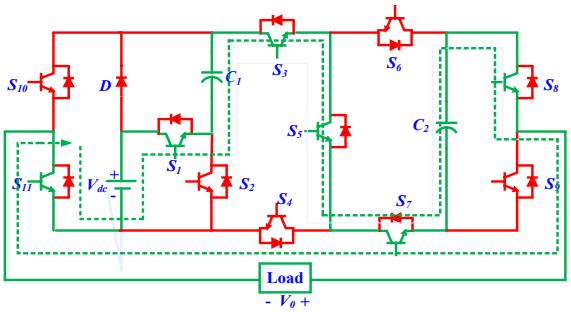
Mode A: In this mode, the source voltage, and capacitors C_1, C_2 are connected to the load through the simultaneous conduction of switches S_1, S_3, S_5, S_7, S_8 and S_{11}. Consequently, the load voltage is $V_0=V_{dc}+V_{C1}+V_{C2}\approx+4V_{dc}$.

Mode B: The load is linked to DC source as well as capacitor C_2 to function this mode of operation. This connection is established due to conductivity of switches D, S_3, S_5, S_7, S_8 and S_{11}. When switch S_2 conducts, capacitor C_1 is

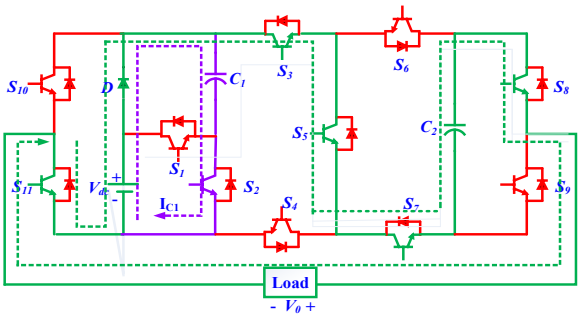
charged, resulting in the load voltage being equal to $V_0=V_{dc}+V_{C2}\approx 3V_{dc}$.

Mode C: The load is linked to the DC source and capacitor C_1 when switches S_1, S_3, S_6, S_8 and S_{11} are turned on. Additionally, capacitor C_2 charges to a reference voltage of $2V_{dc}$ through the conduction of switches S_4, S_5, S_6 and S_7. As a result, the load voltage is $V_0=V_{dc}+V_{C1}\approx 2V_{dc}$.

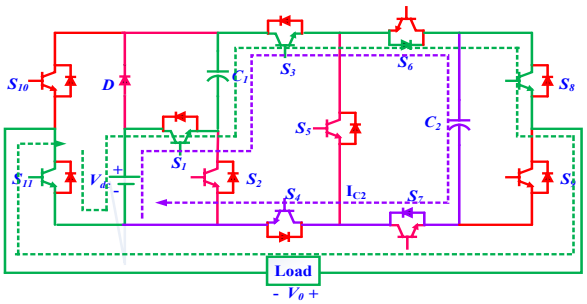
Mode D: The DC source is appearing across the load through switches D, S_3, S_6, S_8 and S_{11}. Additionally, switch S_2 is activated to charge capacitor C_1 to a voltage level of $1V_{dc}$. Capacitor C_2 is left floating (---), it does not charge or discharge. Consequently, the load voltage is $V_0=+1V_{dc}$.



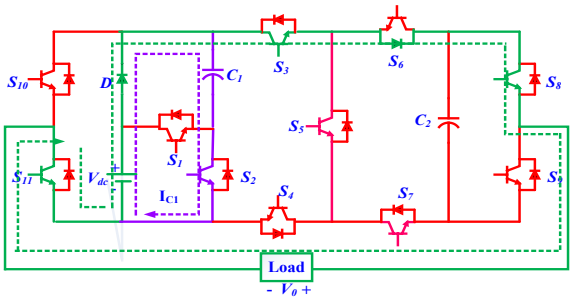
ModeA:$V_0=+4V_{dc}$



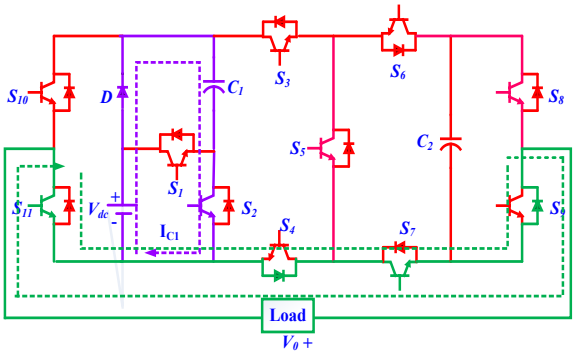
ModeB:$V_0=+3V_{dc}$



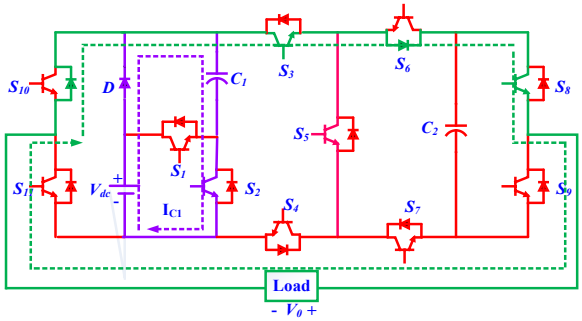
ModeC:$V_0=+2V_{dc}$



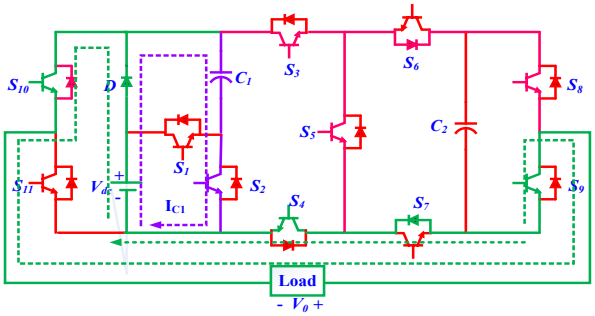
ModeD:$V_0=+1V_{dc}$

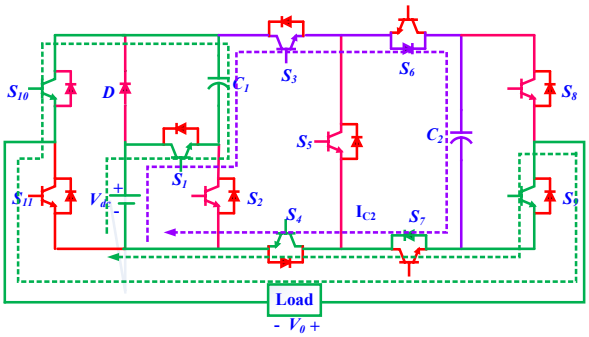


ModeE:$V_0=0$



ModeE:$V_0=0$





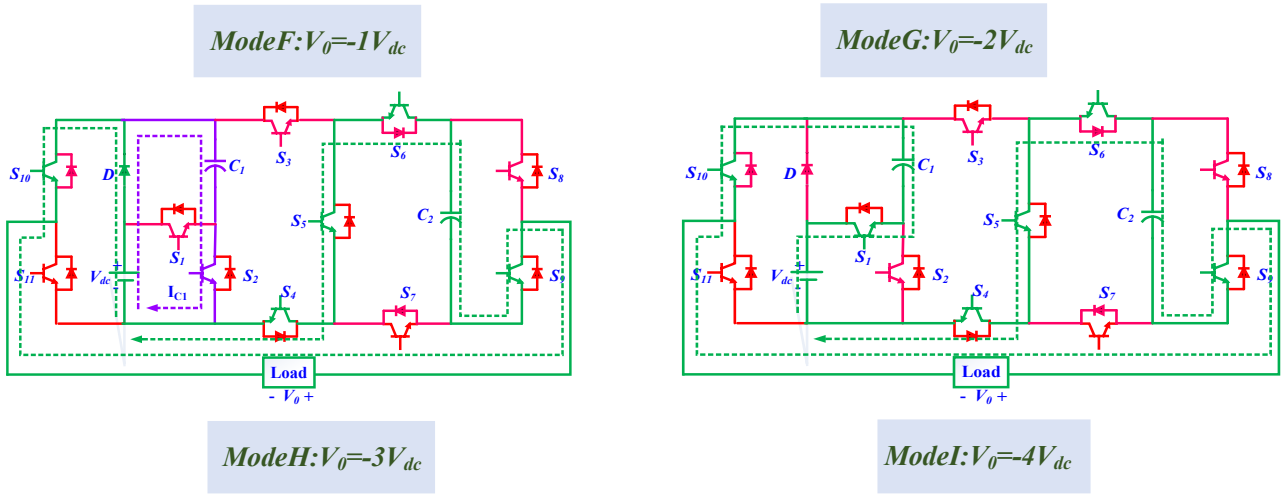


Fig. 3. Operating modes of the topology.

Table 1. Switching modes of nine-level topology

Mode	S_1-S_{11}	V_0	C_1	C_2
A	*10101011001*	$+4V_{dc}$	*D*	*D*
B	*01101011001*	$+3V_{dc}$	*C*	*D*
C	*10110111001*	$+2V_{dc}$	*D*	*C*
D	*01100101001*	$+1V_{dc}$	*C*	---
E	*01010010101*	*0*	*C*	---
F	*01010010110*	$-1V_{dc}$	*C*	---
G	*10110110110*	$-2V_{dc}$	*D*	*C*
H	*01011100110*	$-3V_{dc}$	*C*	*D*
I	*10011100110*	$-4V_{dc}$	*D*	*D*

Mode E: In reality, there are two viable methods to achieve zero voltage in the proposed configuration: either by activating the upper switches (S_3, S_4, S_8 and S_{10}) or the lower switches (S_5, S_8, S_{10} and S_{12}). By enabling the conduction of switch S_2, capacitor C_1 is charged.

Mode F: In this mode source is in series with the load through switches *D*, S_4, S_7, S_9 and S_{10}.Additionally, switch S_2 is activated to charge capacitor C_1 to a voltage level of V_{dc}. Capacitor C_2 is left floating (---), without any charge or discharge. Consequently, the load voltage is $V_0=-1V_{dc}$.

Mode G: Upon activating switches S_1, S_4, S_7, S_9 and S_{10}, the load is linked to the source and capacitor C_1. Additionally, utilizing the conduction of switches S_4, S_5, S_6 and S_7, the capacitor C_2 is charged to a voltage of $2V_{dc}$. Consequently, the load voltage is $V_0=-(V_{dc}+V_{C1}) \approx -2V_{dc}$.

Mode H: The load is connected to the source and capacitor by utilizing the conductive path of switches *D*, S_4, S_5, S_6, S_9 and S_{10}. Capacitor C_1 is charged by activating S_2. Consequently, the load voltage is $V_0=-(V_{dc}+V_{C2}) \approx -3V_{dc}$.

Mode I: To establish a series connection between the source and capacitors C_1 and C_2 to load, switches S_1, S_4, S_5, S_8, S_9 and S_{10} are activated. During this process, both capacitors release their stored energy, supplying $V_0=-(V_{dc}+V_{C1}+V_{C2}) \approx -4V_{dc}$ across the load.

The suggested topology utilizes active switches for each output voltage level. Employing a series-parallel approach, the configuration ensures the self-balancing of capacitors C_1 and C_2. During modes *B, D, E, F* and *H* the capacitor C_1 and DC source operate in parallel, energizing to a voltage of V_{dc}. Conversely, when capacitor C_1 in series with source, it leads to de-energizing capacitor. However, by linking in parallel with the series linkage of C_1 and the source, it helps in energizing to the required voltage level during operating modes *C* and *G*. Capacitors C_1 and C_2 are charged and discharged, respectively, to achieve expected output of $3V_{dc}$. Ultimately, both capacitors discharge to $4V_{dc}$ to balance the system.

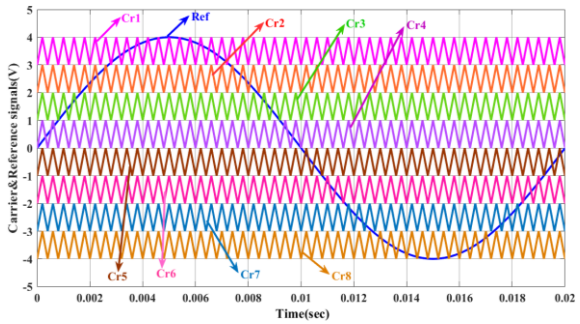


Fig. 4. LSPWM scheme.

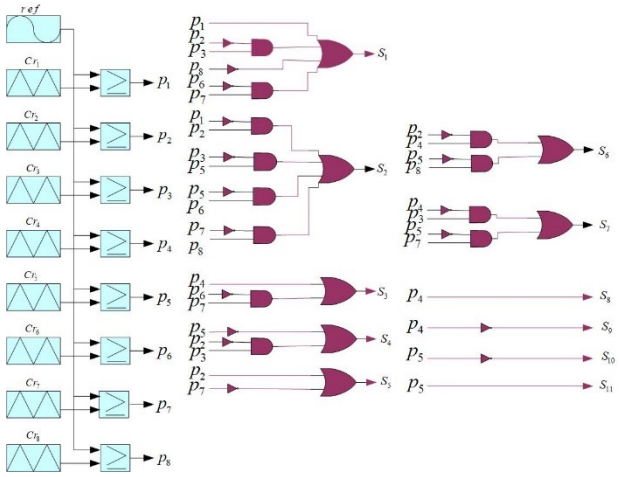


Fig. 5. PWM logic.

2.3. Modulation Scheme

LSPWM scheme utilized for the suggested structure is illustrated in figure4. To offer gating pulses to devices, eight carrier waves and one reference wave are needed. Gate pulses are generated by comparing the reference with carrier waves. Modulation index (m_a) for this topology is expressed as

$$m_a = \frac{A_{ref}}{8A_{cr}} \tag{1}$$

where A_{ref}, A_{cr} are magnitude of reference and carrier waves respectively.

After comparison of reference signal and carrier waves, eight pulses are developed. The positive half cycle pulses are created by utilizing comparison of reference wave and carrier waves Cr_1, Cr_2, Cr_3 and Cr_4 respectively. Likewise, for negative half cycle pulses are developed using Cr_5, Cr_6, Cr_7 and Cr_8 respectively. These eight pulses deliver switching signals to switches (S_1-S_{11}) by employing logic shown in Table 1 and depicted in figure 5.

The maximum inverse voltage (PIV) for each switch for the recommended arrangement seems below $2V_{dc}$.Relying on the operating mode, the switches S_8, S_9, S_{10} and S_{11} work in either positive mode or negative mode. This leads to minimal switching losses of the fundamental frequency operating switches (S_8, S_9, S_{10} and S_{11}). With the aid of Table2, it represents that suggested design provides balanced voltage of capacitors at minimal modulation indices also since the paths for energizing capacitors exist at lower voltage levels, such as 0(for C_1), $\pm 1V_{dc}$ (for C_1) and $\pm 2V_{dc}$ (for C_2). Furthermore, for range of 0.6 to 1, all semiconductor devices are utilized to their full capacity.

3. Capacitor Calculation, Analysis of Switches Ratings and Losses

3.1. Calculation of Capacitors

The capacitance values must be calculated to achieve the expected voltage levels while maintaining acceptable voltage ripples. The total energy utilized to either charging or discharging the capacitors is instrumental in creating the expected levels. In this topology, capacitor C_1 discharges at $\pm 2V_{dc}$ and $\pm 4V_{dc}$ output voltage levels, respectively. Similarly, the other capacitor C_2 discharges at $\pm 3V_{dc}$ and $\pm 4V_{dc}$ output voltage levels, respectively. The maximum allowable discharge (ΔQ_{C1}) required to maintain satisfactory voltage ripple (ΔV_c) for supplying the load resistance (R_L) and fundamental frequency (ω_m) is denoted as

$$\Delta Q_{C_1} = C_1 * \Delta V_{C_1}$$

$$= \int_{\frac{\theta_1}{\omega_m}}^{\frac{\theta_2}{\omega_m}} \frac{2V_{dc}}{R_L} dt + \int_{\frac{\theta_3}{\omega_m}}^{\frac{\pi-\theta_3}{\omega_m}} \frac{3V_{dc}}{R_L} dt + \int_{\frac{\pi-\theta_2}{\omega_m}}^{\frac{\pi-\theta_1}{\omega_m}} \frac{2V_{dc}}{R_L} dt \tag{2}$$

$$\Delta Q_{C_1} = \frac{V_{dc}}{\omega_m R_L}\left(3\pi - 6\theta_3 + 4\theta_2 - 4\theta_1\right) \tag{3}$$

$$\Delta Q_{C_2} = C_2 * \Delta V_{C_2} = \int_{\frac{\theta_3}{\omega_m}}^{\frac{\pi-\theta_3}{\omega_m}} \frac{3V_{dc}}{R_L} dt \tag{4}$$

$$\Delta Q_{C_2} = \frac{3V_{dc}}{\omega_m R_L}\left(\pi - 2\theta_3\right) \tag{5}$$

$$\theta_1 = \sin^{-1}\left(\frac{A_{cr_1}}{A_{ref}}\right) \tag{6}$$

$$\theta_2 = \sin^{-1}\left(\frac{A_{cr_2}}{A_{ref}}\right) \quad (7)$$

$$\theta_3 = \sin^{-1}\left(\frac{A_{cr_3}}{A_{ref}}\right) \quad (8)$$

Considering allowable ripple voltage limit as 10%, C_1 and C_2 are expressed as

$$C_1 \geq \frac{10}{\omega_m R_L}\left(3\pi - 6\theta_3 + 4\theta_2 - 4\theta_1\right) \quad (9)$$

$$C_2 \geq \frac{30}{\omega_m R_L}\left(\pi - 2\theta_3\right) \quad (10)$$

Table 2. Modulation index impact on proposed configuration

Modulation Index	*Level of generation*	*Missing Voltage levels*	*Capacitor Charging*		*Operating switches*
			C_1	C_2	
>0.8	9	*None*	*Yes*	*Yes*	All switches
0.6 to 0.8	7	$\pm 4V_{dc}$	*Yes*	*Yes*	All switches
0.3 to 0.6	5	$\pm 4V_{dc}, \pm 3V_{dc}$	*Yes*	*Yes*	All switches except S_5

3.2. Analysis of Switches Ratings

In the proposed topology, the complementary devices (S_8, S_9, S_{10} and S_{11}) experience the same peak voltage stress, while (S_3, S_4, S_5, S_6 and S_7) exhibit similar peak voltages as their complementary switches. The switches (D, S_1, S_2) operates at minimal peak voltages in contrast to others. The maximum voltage stress on the switching devices is represented as equations (11), (12), and (13) respectively, where V_{Sn} corresponds to the peak voltage related to the respective switch when it is turn-off. The Total Standing Voltage (TSV) for this work is indicated as equation (14).

$$V_{S_8} = V_{S_9} = V_{S_{10}} = V_{S_{11}} = V_{C_2} = 2V_{dc} \quad (11)$$

$$V_{S_3} = V_{S_4} = V_{S_5} = V_{S_6} = V_{S_7} = V_{C_2} = 2V_{dc} \quad (12)$$

$$V_D = V_{S_1} = V_{S_2} = V_{C_1} = V_{dc} \quad (13)$$

$$TSV = 3*V_{S_1} + 9*V_{S_4} = 21V_{dc} \quad (14)$$

The TSV (p.u.) represents the proportion of the cumulative peak inverse voltages of devices to maximum voltage of load. The TSV (p.u.) is calculated for proposed design is to be 5.25 p.u. The voltage stress experienced by all devices at different levels is illustrated as bar chart shown in figure 6. Referring to Table 1, at a particular voltage $+4V_{dc}$, devices S_1, S_3, S_5, S_7, S_8, S_9 and S_{11} are conducting while other switches are in the off condition. Therefore, the voltage stress of D and S_2 is $1V_{dc}$, while on S_4, S_6 and S_{10} are $2V_{dc}$ respectively, as depicted in figure 6. For level $+3V_{dc}$, the voltage stress on devices S_1 is $1V_{dc}$, and for S_5, S_7, S_{10}, S_{11} is $2V_{dc}$, as illustrated in figure 6. Similarly, switching devices voltage stress for other levels is presented in figure 6.

Utilizing the switching states outlined in Table 1, the current ratings of semiconductor devices are estimated and presented in Table 3. Six devices are solely responsible for handling the load current and, therefore, should be designed for the peak value of the load current (I_0). Additionally, five devices are required to handle both load current and capacitor (C_2) currents, while one device is designated to handle the capacitor (C_1) current exclusively. These currents are calculated using equations (15), (16), and (17). The voltage drops V_{sn}, and R_{sn} correspond to the on-state voltage drop of devices and on-state resistance respectively. When determining the output parameters, fundamental computations are performed to configure the proposed setup for a specific application, considering the ratings of semiconductor devices and capacitor values. The design methodology is illustrated in figure 7.

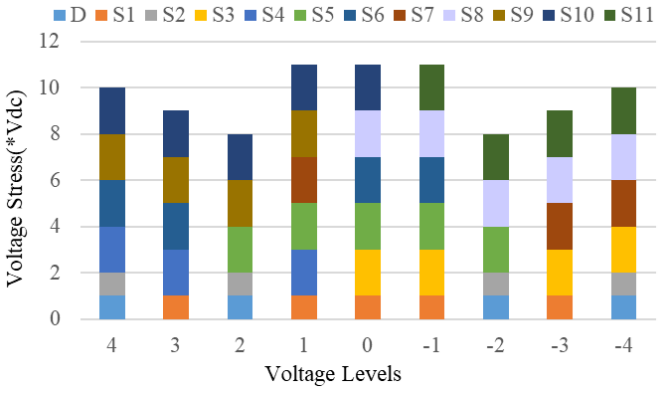


Fig. 6. Bar chart representation.

$$I_0 = \frac{\sqrt{2}P_L}{4mV_{dc}} \quad (15)$$

$$I_{C1} = \frac{V_1}{R_1} e^{-\frac{t}{R_1 C_1}} \quad (16)$$

$$I_{C2} = \frac{V_2}{R_2} e^{-\frac{t}{R_2 C_2}} \tag{17}$$

where

$$V_1 = V_{dc} - V_{S3} - V_{C1}$$

$$R_1 = R_{S3} + R_{C1}$$

$$V_2 = V_{dc} - V_{S1} - V_{S4} - V_{S5} - V_{S8} - V_{C2}$$

$$R_2 = R_{S1} + R_{S4} + R_{S5} + R_{S8} + R_{C2}$$

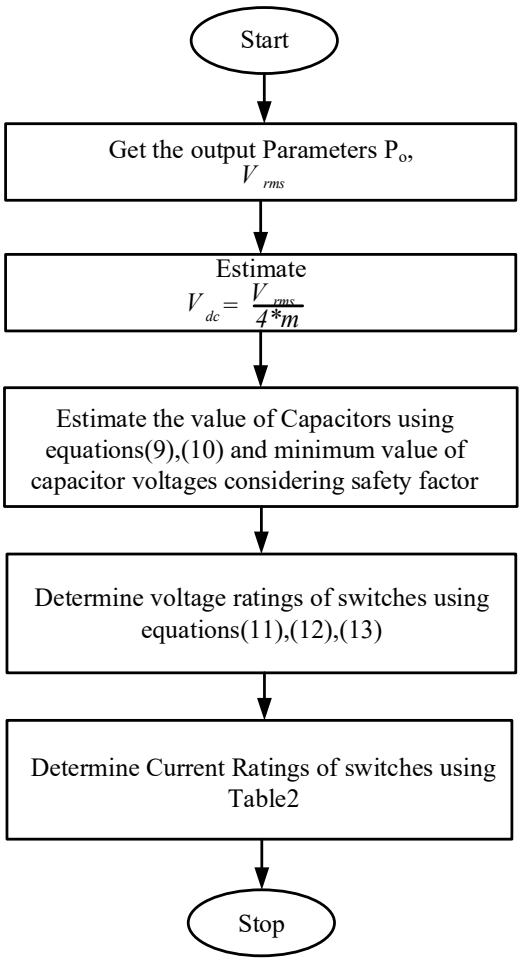


Fig. 7. Design methodology.

Table 3. Current ratings of semiconductor devices

S.No.	Current rating	Semiconductor Devices
1	I_0	S_2, S_6, S_9, S_{10}, S_{11}, S_{12}
2	I_{C1}	S_3
3	$I_{ac}+I_{C1}+I_{C2}$	S_1, S_4, S_5, S_7, S_8

3.3. Loss Analysis

The inverter's efficiency is usually presented as equation (18)

$$\eta = \frac{P_{out}}{P_{in}} * 100 = \frac{P_{out}}{P_{out} + P_{losses}} * 100 \tag{18}$$

where P_{out}, P_{in}, P_{losses} represents power output, power input and power losses respectively.

The power losses in the proposed topology can be categorized into switching losses, conduction losses, and losses due to capacitor voltage ripple during charging.

Switching losses: These losses occur due to rapid switching on and off the devices within a single cycle. The switching losses resulting from transitions are expressed using the equation

$$P_{swlturnon}(i) = f_{carrier} \int_0^{t_{on}} v(t) i(t) dt$$

$$= f_{carrier} \int_0^{t_{on}} \left(\left(\frac{V_{swoff,i}}{t_{on}} (t_{on} - t) \right) \left(\frac{i_{on,i}}{t_{on}} t \right) \right) d\,t$$

$$= \frac{1}{6} f_{carrier} * V_{swoff,i} * i_{on,i} * t_{on} \tag{19}$$

$$P_{swlturnoff}(i) = f_{carrier} \int_0^{t_{off}} v(t) i(t) dt$$

$$= f_{carrier} \int_0^{t_{off}} \left(\left(\frac{V_{swoff,i}}{t_{off}} t \right) \left(\frac{i_{off,i}}{t_{off}} (t_{off} - t) \right) \right) dt$$

$$= \frac{1}{6} f_{carrier} * V_{swoff,i} * i_{off,i} * t_{off} \tag{20}$$

In this context $P_{swlturnon}(i)$, $P_{swltunoff}(i)$ and V_{swoff} represent the ith switch's turn-on loss, turn-off loss, and off-state voltage, respectively. The currents during the switch's on- and off-states are denoted as I_{on} and I_{off} respectively. The total switching losses (P_{sw}) are calculated by summing these losses, as demonstrated in Equation (19).

$$P_{sw}(Total) = \sum_{i=1}^{N_{sw}} \begin{pmatrix} \sum_{j=1}^{N_{on}(i)} P_{swlon}(ij) + \\ \sum_{j=1}^{N_{off}(i)} P_{swloff}(ij) \end{pmatrix} \tag{21}$$

Conduction losses: The conduction losses in a switch and are expressed as

$$P_{swcon} = V_{swon} * i_{swavg} + R_{swon} * i_{swrms}^2 \tag{22}$$

$$P_{Dcon} = V_{Don} * i_{Davg} + R_{Don} * i_{Drms}^2 \tag{23}$$

where P_{Dcon} and P_{swcon} are diode and switch conduction losses, V_{don} and V_{swon} are on-state voltage drop of diode, switch respectively. R_{Don} and R_{swon} are on-state resistance of diode and switch, i_{Davg}, i_{swavg}, i_{Drms} and i_{swrms} are average and RMS currents of switch respectively.

Capacitor voltage losses: When there is a voltage variation between the DC source and the capacitors, power losses (PCloss) occur due to the capacitors. These losses in a parallel combination of the source and capacitors are expressed in Equation (24)

$$P_{Closs} = \frac{1}{2} \sum_{k=1}^{n} C * \Delta V_k^2 * f_{ref} \tag{24}$$

where ΔV_k, f_{ref} represents voltage ripple of capacitor and reference frequency respectively. As a result, the outcome of losses is sum of all losses represented in Equation (25)

$$P_{Total}(loss) = P_{swloss} + P_{conloss} + P_{Closs} \quad (25)$$

4. Results and Discussions

4.1. MATLAB/Simulink Results

To model the performance of the suggested design, MATLAB/Simulink is employed. Table 4 lists the simulation components: source voltage, capacitor voltages are set at 100V, 100V, and 200V, respectively. The load parameters for this study include a 100 Ω resistance, 100mH inductance, and 2200µF for both capacitors. The inverter operating frequency is 50Hz.

Table 4. Simulating parameters

Components	Values
DC source	100V
Capacitor Voltages (V_{c1}&V_{c2})	100V,200V
Resistance	100Ω
Inductances	100mH,150mH, 200mH
Capacitor(C_1&C_2)	2200µf
Reference frequency	50Hz
Carrier frequency	5kHz

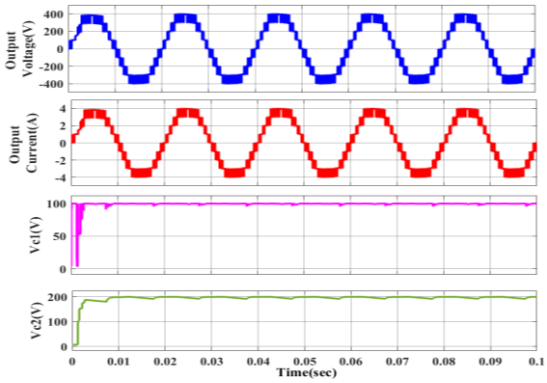


Fig. 8. Output voltage, current and capacitor voltages for R-load.

The inverter operation for an R-load is depicted in figure 8. The output current waveform appears like the output voltage waveform. Figure 9 displays the waveforms for the nine-level inverter under various load conditions. The load voltage remains constant regardless of the load variations. However, the current waveform is zero during on no load, it follows the voltage for resistive loads and lags for inductive loads. Figure 10 exhibits waveforms concerning the variation of output impedance. It is observed that an increase in inductance results in a decrease in current amplitude. Consequently, a higher inductive load leads to more lagging current. Figure 11 illustrates the output waveforms for modulation index regulation (m_a).

In Figure 11, eight carriers contrast with one reference for modulation indices of 1 and 0.9. However, the width of the resultant waveform is minimized for 0.9. Similarly, for modulation indice of 0.7, the operation shifts to that of a seven-level inverter, with a reduction in peak value. For modulation index values of 0.6 and 0.4, it behaves as a five-level inverter. Likewise, for modulation indice of 0.2, the inverter functions as a three-level. The capacitor voltages remain constant at 100V for C_1 and 200V for C_2.

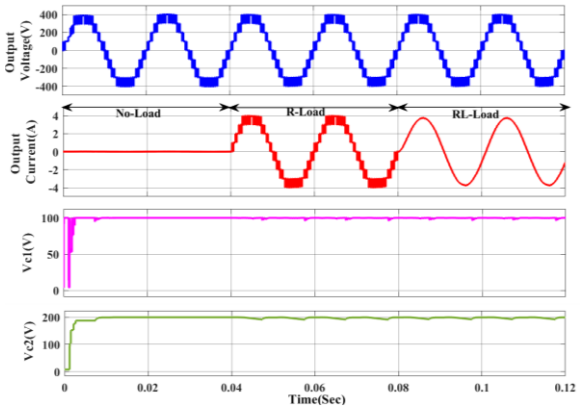


Figure 9. Output voltage, current and capacitor voltages for various Loading conditions

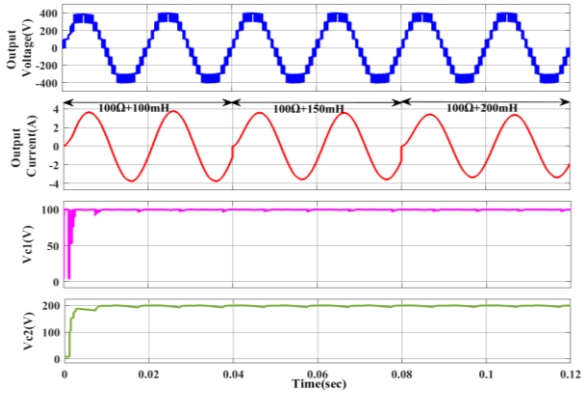


Figure 10. Output voltage, current and capacitor voltages for various RL-loads.

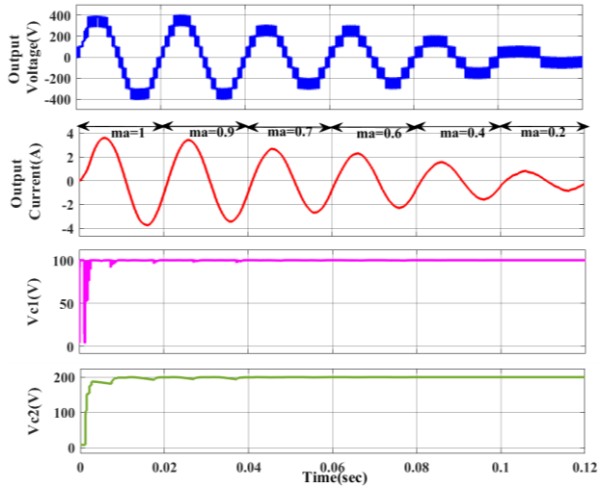


Fig. 11. Output voltage, current and capacitor voltages for variation in modulation index.

Figure 12 displays the resulting waveforms for the regulation of the reference frequency. It is observable that increasing the reference frequency causes a decrease in load

current when load impedance is increased. The proposed configuration proves to be suitable for high-frequency operating loads. In figure 13, output waveforms are depicted for modifications in the carrier frequency($f_{carrier}$). As the carrier frequency fcarrier increases, switching losses escalate due to the increased pulse count for each level. Consequently fcarrier, is limited to a specific value to control THD and size of filter. For this study, the carrier frequency is assumed to be 5kHz.

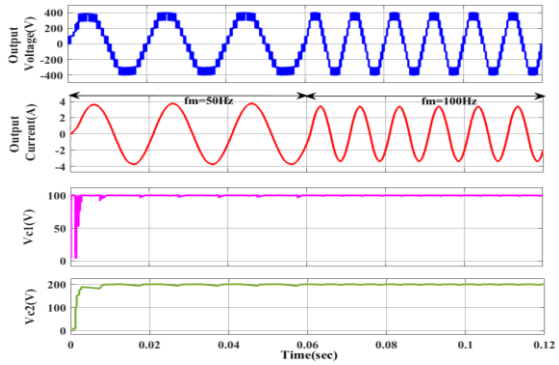


Fig. 12. Output Voltage, Current and capacitor voltages for variation in reference frequency.

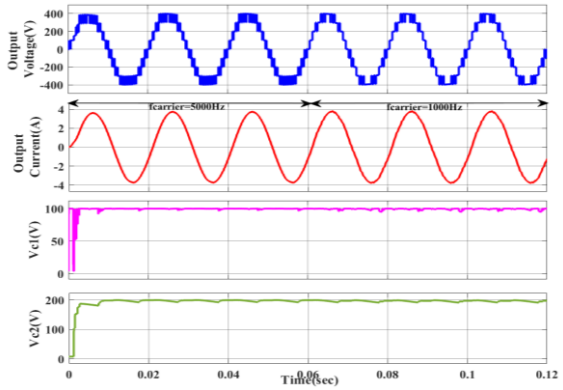


Fig. 13. Output Voltage, Current and capacitor voltages for variation of carrier frequency.

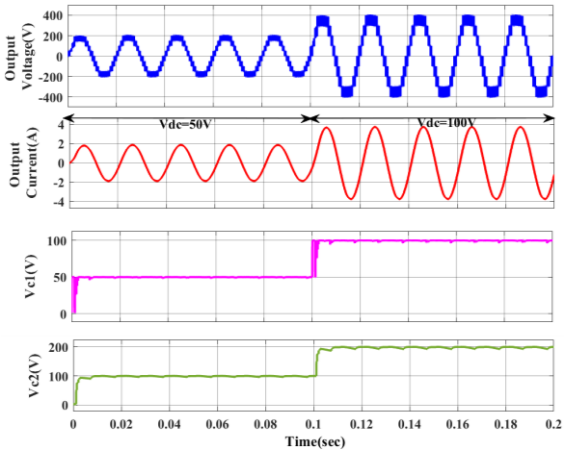
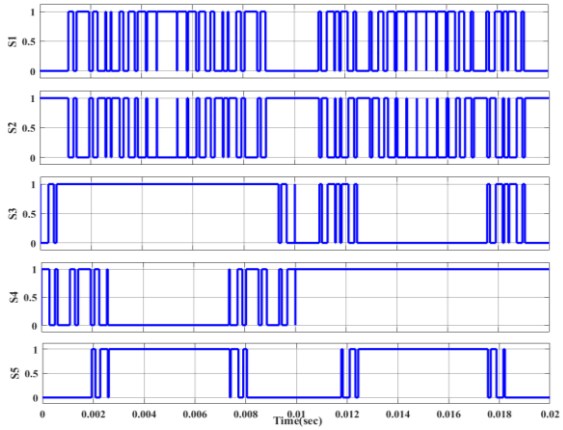
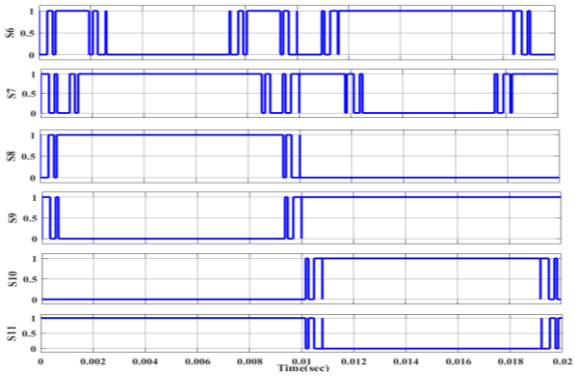


Fig. 14. Output Voltage, Current and capacitor voltages for variation of Source voltage.

When input voltages are varied to 50V and 100V, the corresponding waveforms are observed and illustrated in figure 14. The output voltage maintains its nine-level configuration; however, the amplitudes of voltage and current undergo changes. Specifically, capacitor C_1 is balanced at 50V and 100V, and the capacitor voltage C_2 is balanced at 100V and 200V. The modes of operation for the switches within one cycle are considered and depicted in Figure 15.



(a). switches S_1-S_5



(b). switches S_6-S_{11}

Fig. 15. Switching pulses.

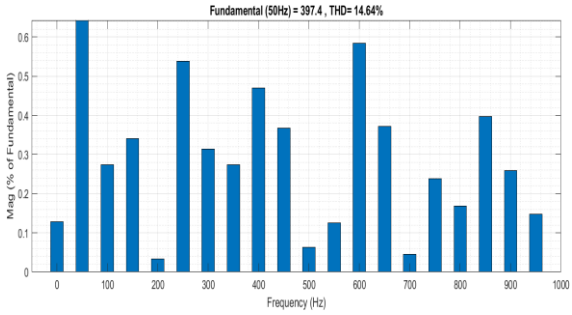


Fig. 16. THD of the output voltage.

Total Harmonic Distortion (THD) of the proposed configuration is 14.64% with a fundamental magnitude of 397.4 volts is illustrated in figure 16. The relationship between modulation indices and THD (%) as well as fundamental output is shown in figure 17. It seems that reducing the modulation index results in a lower amplitude of the fundamental and a higher THD (%). Based on simulation results, proposed topology is found to be suitable for all load conditions.

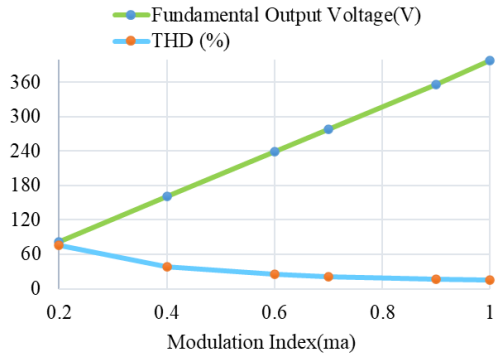
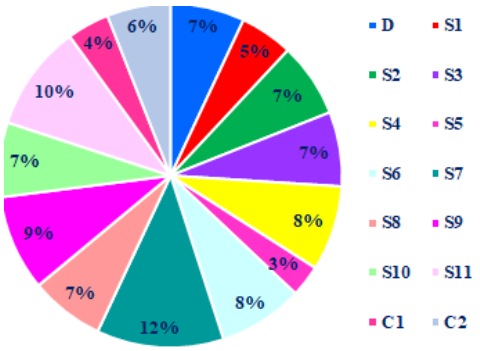
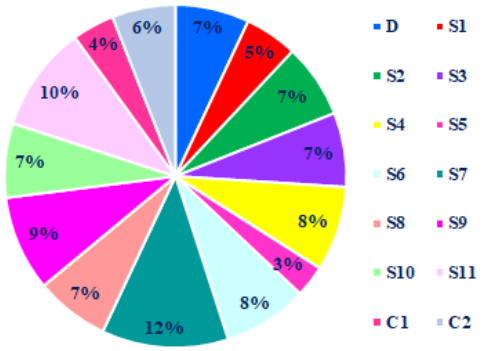


Fig. 17. THD and fundamental component analysis for various modulation indices.



(a). For R-load.



(b). For RL-load.

Fig. 18. % of total losses across switches under various loads.

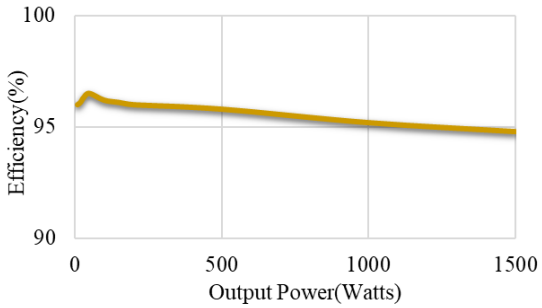


Fig. 19. Efficiency versus output power (Watts).

4.2. Thermal Modelling

PLECS software is utilized to create a thermal model for the power semiconductor devices in the proposed configuration. In figures 18(a) and 18(b), the percentage of losses for semiconductor devices is depicted under loading conditions of 100Ω and 100Ω+100mH, respectively. Efficiency calculations were carried out for loads ranging from 0 to 1500W, and the results, as shown in figure 19, demonstrate an efficiency range of 96.5% to 95.0%.

4.3. HIL Implementation

A real-time simulator plays a crucial role in designing and validating system effectiveness and accuracy, as models built in real-time operate at the same pace as real systems. The OPAL-RT simulator interfaces with the Sim Power System in MATLAB/Simulink using RT-LAB software. The OPAL-RT RT-LAB platform, equipped with advanced Intel processors and FPGA chips, is integrated into the OP4510 system, providing real-time simulation capabilities.

This multi-rate FPGA-based architecture enables users to model power converters for Hardware-in-Loop (HIL) applications with time steps as short as 7 µs on INTEL CPU-based sections and even fewer nanoseconds on the FPGA chip. An advanced PWM controller is capable of real-time hardware regulation, offering Quick Control Modelling (QCM) services with timing improvements of over 20 nanoseconds. The OP4510 can also function as an independent semiconductor device test system using pre-established models. The implementation of proposed configuration through OP4510 is illustrated in figure 20 and described in detail in this section.

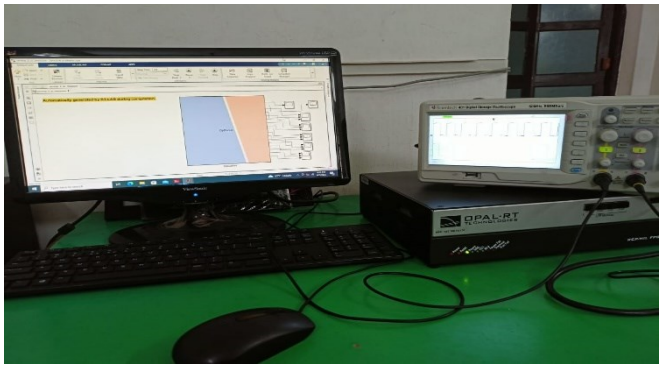
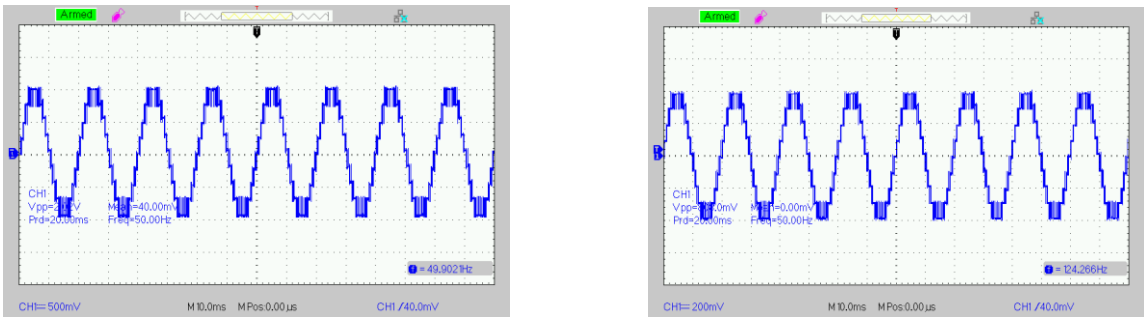


Fig. 20. OPAL-RT test bench.

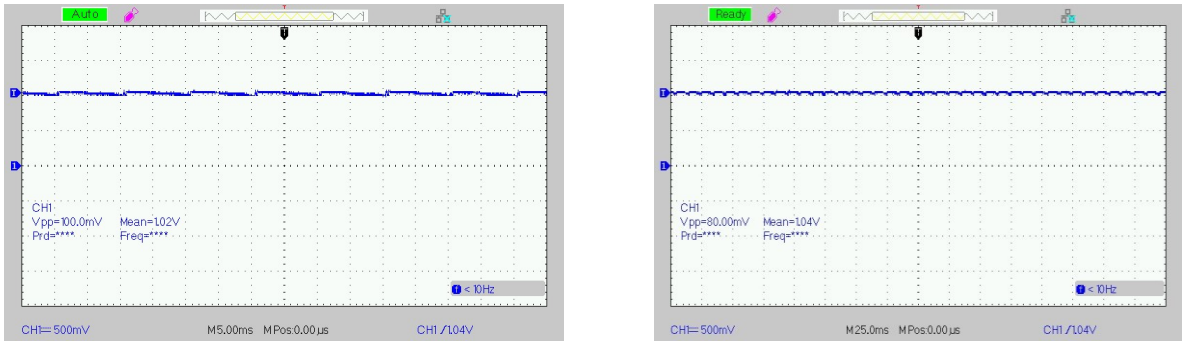
Considering a switching frequency of 5 kHz, the waveforms for loads of 100Ω and 100Ω + 100mH are illustrated in figure 21. As observed in figure 21, the output current follows the voltage for resistive loads and lags in the case of inductive loads. The voltage across two capacitors are shown in figure 22. It is apparent that the real-time simulated outcomes closely match the simulated results obtained through MATLAB/Simulink. The switching pulses for all the switches are presented in figure 23. These real-time results show that the proposed configuration performs effectively across capacitors without the need for additional regulation methods.



(a). Output voltage (b). Output current for R-load

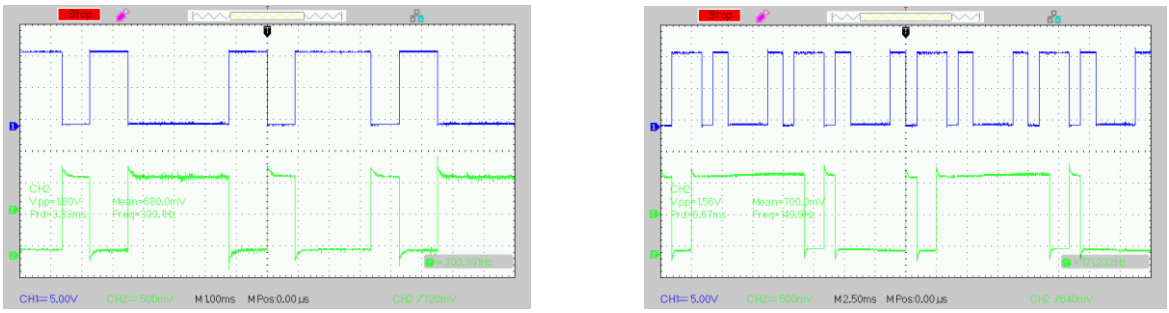
(c).Output current for RL-load

Fig. 21. Output voltage and current

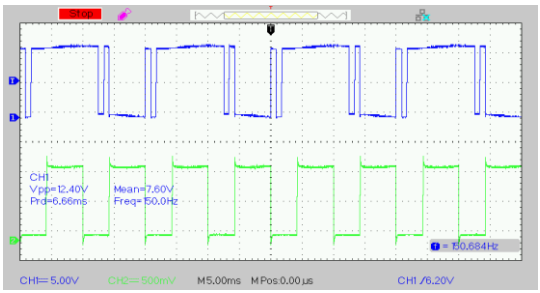


(a). Capacitor C_1 (b). Capacitor C_2

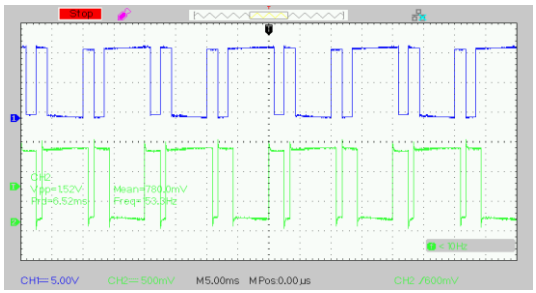
Figure 22. Voltage across capacitors.



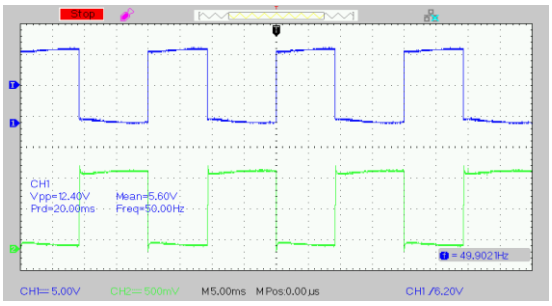
(a). (S_1-S_2) (b). (S_2-S_3)



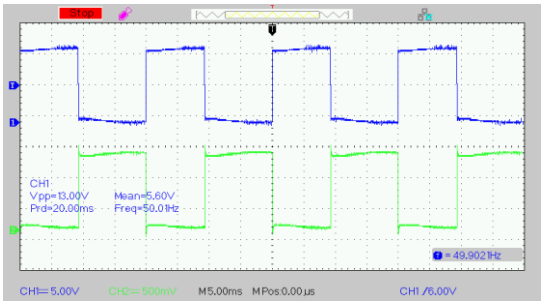
(c). (S_4-S_5)



(d). (S_6-S_7)



(e). (S_8-S_9)



(f). (S_{10}-S_{11})

Fig. 23. Switching pulses.

Table 5. Comparison with other topologies

Topology	N_s	N_{Sw}	$N_{drivers}$	V_C		N_D	N_C	G	*TSV (p.u.)*	*C.F.*	*Voltage Level*	*Efficiency*
				$1V_{dc}$	$2V_{dc}$							
[15]	*1*	*13*	*13*	*3*	*0*	*0*	*3*	*4*	*6.25*	*36.25*	*9*	*85.9%*
[16]	*1*	*12*	*12*	*3*	*0*	*2*	*3*	*4*	*6.25*	*35.25*	*9*	*83%*
[18]	*1*	*8*	*8*	*3*	*0*	*6*	*3*	*4*	*8*	*34*	*9*	*91.5%*
[21]	*1*	*10*	*10*	*3*	*0*	*3*	*3*	*4*	*6.25*	*33.25*	*9*	*91.6%*
[25]	*1*	*10*	*10*	*3*	*0*	*4*	*3*	*4*	*7.5*	*34.25*	*9*	*93.5%*
[26]	*1*	*17*	*17*	*4*	*0*	*0*	*4*	*4*	*7.25*	*46.25*	*9*	*NA*
[27]	*1*	*18*	*18*	*4*	*0*	*5*	*4*	*4*	*7*	*53*	*9*	*92.5%*
[41]	*1*	*12*	*11*	*3*	*0*	*0*	*3*	*4*	*6.5*	*33.25*	*9*	*90%*
[28]	*1*	*12*	*12*	*4*	*0*	*0*	*4*	*4*	*12*	*41*	*9*	*96%*
[29]	*1*	*16*	*16*	*3*	*0*	*0*	*3*	*4*	*7*	*43*	*9*	*NA*
[30]	*1*	*12*	*11*	*4*	*0*	*2*	*4*	*4*	*7.5*	*37.5*	*9*	*94.5%*
[10]	*1*	*14*	*14*	*5*	*0*	*0*	*5*	*4*	*7.5*	*41.5*	*9*	*95%*
[32]	*1*	*9*	*9*	*5*	*0*	*2*	*5*	*4*	*10*	*36*	*9*	*94%*
[36]	*1*	*12*	*12*	*3*	*0*	*1*	*3*	*4*	*7.5*	*35.5*	*9*	*87%-95%*
Proposed	***1***	***11***	***11***	***1***	***1***	***0***	***2***	***4***	***5.25***	***32.25***	***9***	***96.5%***

4.4. Comparison

Table 5 compares different configurations with the suggested configuration relying on the number of sources (N_s), switch count (N_{sw}), number of gate driver circuits ($N_{drivers}$), diodes count (N_D), capacitor count (N_C), cost factor (CF), and efficiency. The cost factor is calculated using the expression given in Equation (26).

$$CF = N_s + N_{sw} + N_{drivers} + N_D + N_C + \delta * TSV(p.u.) \quad (26)$$

Here, δ represents the weightage factor. A value of δ less than 1 increases the weightage of components, whereas a value of δ greater than 1 gives more weightage to Total Standing Voltage (TSV) (p.u.). If δ equals 1, the weights of components and TSV (p.u.) are identical. For this study, δ is considered as 1.

Upon analysing Table 5, it is evident that [17] ,[41] , [28] ,[36] feature an equal number of switches and exhibit the minimum switch count in comparison to other topologies such as [18] .The increase in the requirement of switches, diodes, and capacitors affects the cost factor, as expressed in Equation (26). Consequently, for [26] , [27] , [28] , [29] and [10] the cost factor is higher than other topologies listed in Table 5. It is noteworthy that [15] , [17] and[21] share equal Total Standing Voltage (TSV) values, while [28] has a higher value and the proposed configuration has minimal value respectively. Considering all these factors, suggested configuration is optimized for generating nine levels.

5. Conclusion

This work outlines a new nine-level quadruple inverter employing a switched capacitor approach, enabling self-balancing of capacitor voltages. The proposed layout is simulated in MATLAB/Simulink, considering various scenarios such as load variations, source voltage fluctuations, modulation index adjustments, reference frequency changes, and carrier frequency variations. The simulation results represents that the suggested configuration is applicable for a wide range of loading conditions. To assess its superior features, the suggested design is compared with existing topologies from the literature. The analysis reveals that the proposed design employs minimal components while maintaining an acceptable TSV. Furthermore, overall efficiency of the configuration is evaluated using PLECS software, which estimates losses in the switches. The efficiency of the proposed design is found to reach up to 96.5%. Finally, the efficient functioning of the topology is validated through Hardware-in-Loop (HIL) testing and outcomes are presented. The results suggested that proposed design shows elegant results.

Acknowledgements

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Author Contributions

Lakshmi Prasanna: Writing – review & editing, Writing – original draft, Validation, Conceptualization. T.R. Jyothsna: Writing – review & editing, Supervision, Formal analysis, Conceptualization. P. Rajagopal: Writing – original draft, Validation, Formal analysis.

Conflict of Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this work.

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