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A UPF DC Fast Charger for Plug-in Electric Vehicles Based on Dual-Stage Configuration

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Abstract- Electric vehicles (EVs) herald a new era of emission-free and eco-friendly mobility while diminishing dependency on fossil fuels. However, their adoption faces hurdles like prolonged charging durations and restricted range, limiting their widespread acceptance. Therefore, fast-charging technology is essential for EV commercialization to overcome these limitations. This paper proposes a simple and cost-effective unity power factor (UPF) DC fast charger (FC) for plug-in EVs, featuring high power quality and short charging time. The proposed FC is considered a dual-stage configuration, operating at UPF without requiring separate power factor correction (PFC) circuitry. This dual-stage configuration consists of two power stages: a 3-phase pulse width-modulated (PWM) rectifier in the input stage and a buck converter in the output stage, resulting in a significantly efficient proposed FC circuit. Also, a control strategy is proposed for the considered FC, specifying two key approaches: voltage-oriented control (VOC) scheme and constant current-constant voltage (CC-CV) charging method. The VOC scheme ensures UPF operation by attaining fast and dynamically regulated DC-bus voltage during EV charging. Meanwhile, the CC-CV charging method effectively manages EV battery charging in different charging modes, minimizing charging duration and preventing overcharging. The proposed control strategy has been validated by simulation software using the MATLAB/Simulink® environment. The simulation outcomes strongly support the efficacy of the proposed control strategy for the considered FC, including achieving a UPF, regulating the DC-bus voltage level with minimal ripple, minimizing harmonic currents though lower total harmonic distortion (THD) of 1.6%, and achieving CC-CV fast-charging.

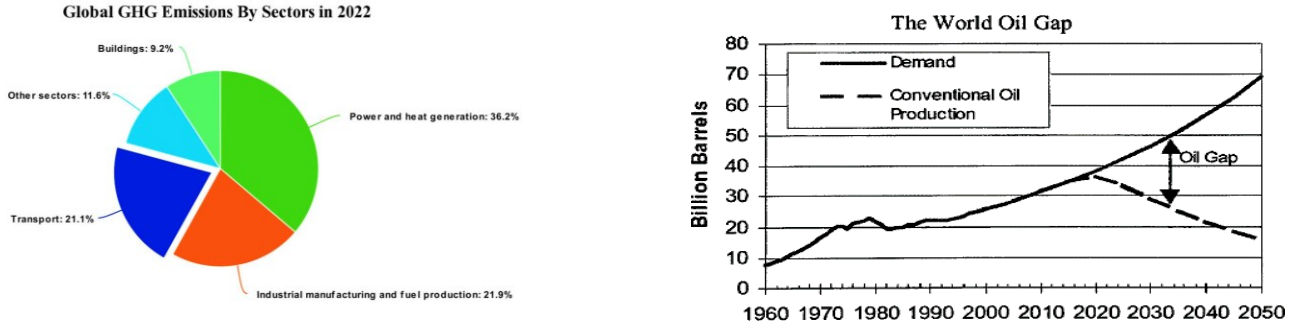
Keywords Electric vehicle, fast charger, battery charging, active front-end rectifier, voltage-oriented control, constant current-constant voltage technique.

1. Introduction

Transportation, an essential aspect of our daily lives, has played a vital role in many particular and commercial activities for centuries. However, the transportation sector, which includes road transportation, non-road transportation, aviation, and inland waterways, is in charge of around 25% of the global emissions of greenhouse gases (GHG), ranking it prominently among the largest GHG-emitting sectors, as shown in Fig. 1(a) [1]. Road transportation alone contributes about 75% of the total transportation emissions, with conventional vehicles being a significant cause of air pollution [2]. Inhaling the particles present in these emissions poses a significant health risk to humans, as some of these particles are cancerous. Beyond environmental and health concerns, a serious problem arises from the dependence on oil resources that may be depleted soon, as conventional vehicles are increasing in parallel with the lower availability of world oil, leading to a potential global economic crisis [3], [4], [5].

Figure 1(b) illustrates the striking difference between fuel demand and world oil production after 2020 [6].

In this regard, electric vehicles (EVs) represent a promising technology that will make a revolution in the transport and energy sectors due to a myriad of compelling features like emission-free, silent operation, low maintenance, high energy efficiency, and appropriate propulsion requirements [7], [8], [9]. Therefore, many countries around the world are shifting towards EVs as the best alternative to conventional vehicles [10], [11]. This shift reflects a collective commitment to mitigating environmental impacts, reducing dependence on finite oil resources, and embracing innovative solutions for sustainable mobility [12]. However, to achieve this shift, EVs suffer from some limitations that should be overcome. Range anxiety, charging facility availability, and relatively extended charging time in comparison to the refueling of conventional vehicles are commonly mentioned as the significant impediments that hinder the broader acceptance of EVs in the market [13]. These challenges, while not insurmountable, are crucial considerations in ensuring the success of the transition to EVs on a global scale. Therefore, to promote the widespread adoption of EVs in the future, it is necessary to design EVs equipped with a fast-charging option. This is crucial to address the significant disparity in refueling times between conventional vehicles and current EV charging methods. Refueling a conventional vehicle typically requires 2 to 5 minutes, whereas an EV recharges the battery pack using residential or public charging options for several hours to drive about a few hundred kilometers per single charge [14]. If the fast-charging technology successfully reduces the replenishing time to levels like the typical refueling time of conventional vehicles and the fast-charging stations become as ubiquitous as traditional gas stations, it would contribute to a substantial increase in the acceptance and popularity of EVs [14], [15].



(a) (b)

Fig. 1. (a) Global GHG emissions attributed to each sector according to the joint research centre (JRC) report 2023 [1], (b) World oil demand by 2050 [6].

Nowadays, a significant step has been taken by EV manufacturers regarding narrowing the gap between EVs and conventional vehicles. This has promoted the advancement of appropriate chargers that can accommodate grid-compliant fast-charging as a viable way to address some of the enunciated issues and make EVs more competitive [16], [17].

Charging levels for EV conductive charging are classified according to the power rating utilized [18]. The Society of Automotive Engineers (SAE) specifies the conductive charging of EVs within the framework of the SAE J1772 Standard [19]. This standard plays a crucial role in ensuring consistency and interoperability across charging infrastructure and EVs. It classifies conductive charging into three different levels (1-2-3), each corresponding to different charging speeds and power levels to accommodate various use cases and charging needs [20]. Level 1 and 2 charging have modest power ratings, making them well-suited for slow charging. Hence, the restricted power levels of these charging levels have prompted the advancement of fast-charging technology. Level 3 charging can be classified as fast-charging because of its external charger and higher power ratings, typically delivering power at 50 kW and, more lately, reaching power ratings of up to 350 kW. In level 3 charging, there is a direct connection between the vehicle batteries and a high-current DC power source. This direct connection allows for a more efficient transfer of electrical energy to the vehicle's battery, enabling faster charging compared to the AC charging used in level 1 and 2 charging. The power source typically takes 30 minutes or less to charge the vehicle's battery to 80% of its capacity [21], [22].

Recently, the EV conductive charging system offers two fundamental options for battery charging: on-board charging and off-board charging, according to the charger position in relation to the vehicle [23]. Hence, two main categories of EV chargers exist. The on-board charger (OBC), occasionally called a slow charger, is situated within the vehicle itself to allow low-power transfer for battery charging while the vehicle is parked and plugged into a charging socket [24]. In contrast, the off-board charger (OFBC), also known as a fast charger (FC) or ultra-FC, is situated outside the EV and

provides a direct high-power rapidly to the batteries [25]. The OBC typically functions at rates of 0.1-0.2C, whereas the OFBC typically achieves rates of 1-2C, where C represents the battery capacity [26]. Therefore, the OBC constrains the power to either level 1 or level 2 due to limitations related to weight, space, and cost considerations. These constraints make the OBC suitable for nighttime charging using a household AC utility outlet or daytime charging at workplaces or shopping centers. Whilst the OFBC, also known as a level 3 charger, can be installed at specialized locations to offer fast-charging services. Figure 2 shows the fundamental diagram of on/off-board chargers with various charging levels [27].

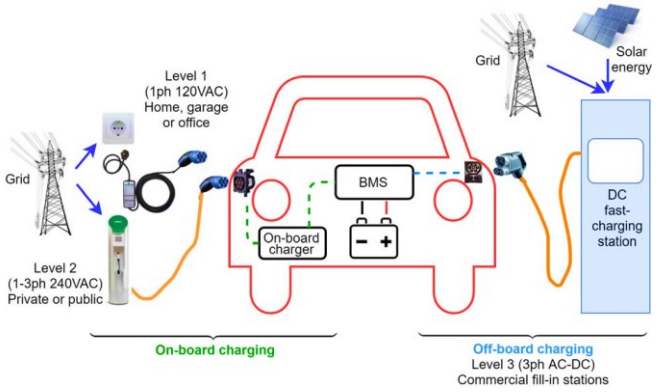


Fig. 2. On/off-board chargers with corresponding charging levels [27].

This paper proposes a unity power factor (UPF) DC FC for plug-in EVs, employing a suggested control strategy that consists of voltage-oriented control (VOC) scheme and constant current-constant voltage (CC-CV) charging method. The proposed FC primarily comprises two stages. The input stage features an active front-end (AFE) pulse width-modulated (PWM) rectifier of the two-level type to perform the role of an intermediary between the DC-bus and the AC grid while meeting the grid standards for power factor (PF) and total harmonic distortion (THD). Meanwhile, the output stage composes a back-end buck converter to carry out the charging operation for the EV battery. This proposed FC, employing a buck-type converter, offers rectification while maintaining a regulated DC output voltage, operating at UPF without requiring separate power factor correction (PFC) circuitry. Additionally, it efficiently manages charging by lowering the DC-bus voltage to be compatible with the EV battery while controlling the injected current.

The subsequent sections are arranged as follows: Section 2 provides an illustration of the proposed FC configuration. Then, Section 3 gives a detailed description of the proposed FC through mathematical modeling and functional operation, explaining the suggested control strategy utilized. To verify the suggested control strategy, Section 4 covers the obtained simulation results. Ultimately, Section 5 concludes this paper.

2. Proposed Fast Charger Configuration

The state-of-the-art FCs typically require a low-frequency (LF) grid transformer, which increases both the size and weight [28], [29]. Another attractive solution is the proposed FC based on a closed-loop DC-DC buck converter using the CC-CV charging method. This buck-type FC provides AC-DC conversion with a controlled DC-bus voltage, guarantees a UPF without requiring separate PFC circuitry, reduces THD caused during charging according to recent power quality regulations [30] that impose restrictions on the harmonics of the current taken from the AC utility, and lowers the DC-bus voltage while monitoring the battery charging. Additionally, it ensures that the undulation in the battery charging current remains within a secure operational range. Figure 3 depicts the block diagram of the proposed FC.

The proposed system model comprises two power stages. The input stage incorporates a 3-phase AC-DC converter tied to the grid via an interfacing AC electromagnetic interference (EMI) filter to act as an AFE PWM rectifier of the two-level type. The output stage comprises a back-end buck converter to interface with the batteries. Both of these converters have gained popularity in industries due to their high efficiency, affordability, and compact size. The popularity of these converters signifies their reliability and acceptance in diverse applications, reinforcing the proposed FC as a cutting-edge solution that aligns with contemporary industry standards and addresses the evolving needs of EV charging systems. Therefore, the combination of these converters results in a significantly efficient circuit for the proposed FC. Both stages are designed to facilitate a rapid battery charging process. As evident, this dual-stage configuration isn't galvanically isolated because the galvanic isolation is only mandatory between the vehicle body and the traction battery, in accordance with the IEC 61851-1 standard [31].

Considering that the AFE PWM rectifier functions as a boost-type converter, the voltage on the DC-bus can vary within a broad range of values; however, it consistently remains higher than the maximum instantaneous phase-to-phase grid voltage. Hence, there is a need to employ a back-end buck converter for regulating the voltage on the DC-bus at a level suitable for the battery charging process (typically, the nominal voltage of EV batteries is less than 560 V_{DC}). The proposed FC comes with many desirable features, including a simple structure, well-established control schemes, a streamlined power conversion setup with fewer electronic components, inherent protection against reverse current from the battery, cost-effectiveness, and compactness.

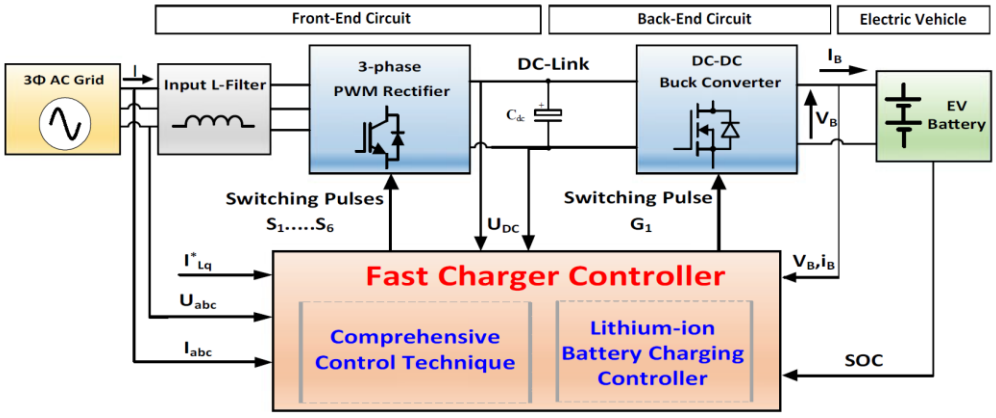


Fig. 3. Block diagram of the proposed FC.

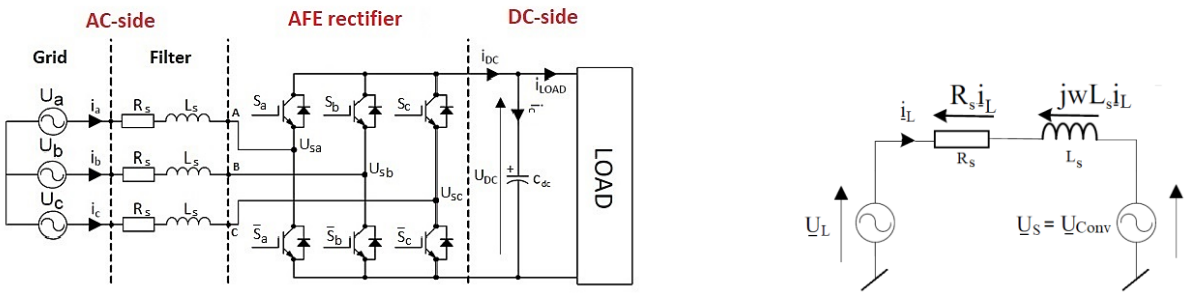
3. Proposed Fast Charger Conversion Scheme: Modeling and Control

3.1. Input Power Stage (AC-DC)

3.1.1. Circuit description and operating analysis

The input stage adopted in this paper is constructed with a 3-phase AFE PWM rectifier of the two-level type that is tied to the electric utility via input L-filters. Specially, L-filters are used on the AC-side due to many advantages, including their simplicity, ease of design, and effectiveness in mitigating PWM harmonics in the grid input current during high switching frequencies [32], [33]. In addition, the PWM rectifier has multiple benefits, including it can transfer power bi-directionally, allows controllable PF adjustment to meet the power quality standards for grid-connected converters, and enables the straightforward regulation of DC-bus voltage [20], [34]. The input current is meticulously managed to synchronize with the grid voltage, and this approach is implemented to enhance the input PF. To achieve UPF operation and low THD, this topology is selected for constructing a cost-effective 3-phase rectifier module with a minimal number of components and reduced conduction losses. The DC-bus voltage is consistently regulated to remain higher than the maximum grid line voltage. Hence, this rectifier acts as a voltage booster.

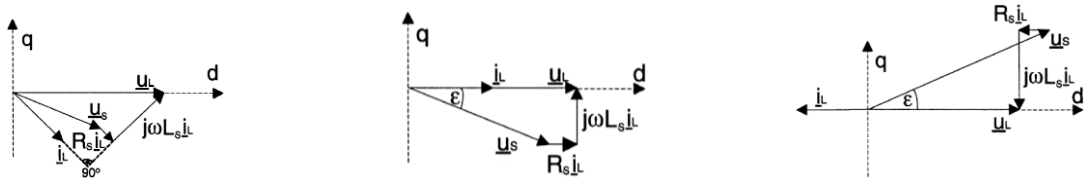
Figure 4(a) shows the basic schematic representation of an AFE PWM rectifier [35]. It comprises three legs (6 IGBTs with anti-parallel diodes) and has a structure in which 2 IGBTs are connected in series to each leg. The two IGBTs on each leg ought to coordinate their operations in a complementary manner. Both IGBTs can be opened at the same time, but it isn't possible to close both IGBTs on one leg simultaneously. If such an event were to transpire, it would result in a short-circuit of the DC-bus, potentially leading to damage to the IGBTs. Hence, a controller is designed to generate an output signal, utilizing a specific modulation technique, for the switching element operation. As shown, the rectifier is tied to 3-phase grid voltages U_a, U_b, and U_c through three inductive filters that have equal inductances L_s and internal resistances R_s. A large DC capacitor C_{dc} is linked across the DC-side U_{DC} for diminishing the DC-bus output voltage oscillations. The circuit depicted is a 3-wire system that lacks a neutral wire. Consequently, it is impossible for zero-sequence current to flow within the circuit, irrespective of the 3-phase voltages applied.



(a) (b)

Fig. 4. (a) Basic schematic representation of an AFE PWM rectifier incorporating an L-filter, (b) Simplified depiction of an AFE PWM rectifier incorporating an L-filter [35].

To ensure effective control of the input stage, it is essential to clearly define the operational principle of the AFE PWM rectifier. Figure 4(b) presents a simplified depiction of the 3-phase PWM rectifier incorporating L-filter [35]. $\underline{U_L}$ represents the line voltage, while $\underline{U_S}$ signifies the rectifier input voltage. The voltage drop on the inductance L_s is utilized to control the line current i_L. This implies that the voltage on the inductance u_l results from the subtraction between the line voltage u_L and the rectifier voltage u_s. Controlling both the amplitude of the rectifier voltage u_s and the phase angle ε indirectly governs both the amplitude and phase of the line current i_L. It will enable control over the sign and average value of the DC current, which are directly proportionate to the useful active power passed via the rectifier. Meanwhile, the reactive power could be autonomously managed through the phase shift between the voltage U_L and the fundamental harmonic current I_L. Figure 5 depicts the phasor diagrams illustrating the PWM rectifier's behavior in various operational modes [36]. Figure 5(a) corresponds to the basic phasor diagram. Figure 5(b) illustrates the rectification operation at UPF, indicating no phase shift between the grid line voltage and the line current. When the grid voltage leads the rectifier voltage, it results in the transfer of active power to the DC-side from the AC-side. Figure 5(c) shows the regeneration operation at UPF, wherein active power moves to the AC-side from the DC-side.



(a) (b) (c)

Fig. 5. Phasor diagrams of an AFE PWM rectifier in various operational modes: (a) Basic phasor diagram, (b) Forward mode under UPF, and (c) Reverse mode under UPF [36].

3.1.2. Mathematical modeling of L-filter based PWM rectifier

The 3-phase PWM rectifier adopted in this paper can be described using a set of four governing equations. Three equations describe phase voltages, while one equation relates to the DC-bus current. By employing Kirchhoff's law of voltage at the AC-side, the voltage differential equations that describe the relation between the rectifier input voltage and the 3-phase AC voltage is formulated in the stationary abc frame for a balanced 3-phase system without the presence of neutral as follows:

$$U_a = R_s i_a + L_s \frac{di_a}{dt} + U_{sa} \tag{1}$$

$$U_b = R_s i_b + L_s \frac{di_b}{dt} + U_{sb} \tag{2}$$

$$U_c = R_s i_c + L_s \frac{di_c}{dt} + U_{sc} \tag{3}$$

where grid voltages are defined as: $U_a = E_m \cos(\omega t)$, $U_b = E_m \cos\left(\omega t - \frac{2\pi}{3}\right)$ and $U_c = E_m \cos\left(\omega t + \frac{2\pi}{3}\right)$, while grid fundamental currents are defined as: $I_a = I_m \cos(\omega t + \varphi)$, $I_b = I_m \cos\left(\omega t - \frac{2\pi}{3} + \varphi\right)$ and $I_c = I_m \cos\left(\omega t + \frac{2\pi}{3} + \varphi\right)$. Here, ω represents the angular frequency, E_m represents the peak value of the phase voltage, and I_m represents the peak value of the phase current.

The Eqs. (1), (2), and (3) can be defined in a different representation using space vectors as follows:

$$\underline{U_L} = \underline{U_i} + \underline{U_{Conv}} \tag{4}$$

$$\underline{U_L} = R_s \underline{i_L} + L_s \frac{d\underline{i_L}}{dt} + \underline{U_{Conv}} \tag{5}$$

$$\begin{bmatrix} U_a \\ U_b \\ U_c \end{bmatrix} = R_s \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + L_s \frac{d}{dt} \begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} + \begin{bmatrix} U_{sa} \\ U_{sb} \\ U_{sc} \end{bmatrix} \tag{6}$$

And since there is no neutral connection here, it's reasonable to assume that the sum of mains currents is zero.

$$I_a + I_b + I_c = 0 \tag{7}$$

According to [35], [36], the PWM rectifier's model can be streamlined to incorporate only three switching states (S_a, S_b, and S_c), where the applied voltage being contingent upon the state (ON/OFF) of the IGBTs. It is acknowledged that, within the same leg of the rectifier, one IGBT switch is always ON while the other one is OFF. Hence, the line-to-line input voltages are expressed as:

$$\begin{aligned} U_{Sab} &= (S_a - S_b) * U_{DC} \\ U_{Sbc} &= (S_b - S_c) * U_{DC} \\ U_{Sca} &= (S_c - S_a) * U_{DC} \end{aligned} \tag{8}$$

Then, the rectifier input phase voltages are equal to:

$$U_{Sa} = f_a * U_{DC}$$
$$U_{Sb} = f_b * U_{DC} \quad (9)$$
$$U_{Sc} = f_c * U_{DC}$$

where f_a, f_b, *and* f_c are the switching functions, which are computed in the following manner:

$$f_a = S_a - S^* = S_a - \frac{1}{3}(S_a + S_b + S_c) = \frac{2S_a - (S_b + S_c)}{3}$$
$$f_b = S_b - S^* = S_b - \frac{1}{3}(S_a + S_b + S_c) = \frac{2S_b - (S_a + S_c)}{3} \quad (10)$$
$$f_c = S_c - S^* = S_c - \frac{1}{3}(S_a + S_b + S_c) = \frac{2S_c - (S_a + S_b)}{3}$$

where f_a, f_b, and f_c are assumed to be 0, ±1/3, ±2/3.

According to the above Eqs. (1), (2), and (3), the AC-side can be modeled as:

$$U_a = R_s i_a + L_s \frac{di_a}{dt} + \frac{2S_a - (S_b + S_c)}{3} * U_{DC} \quad (11)$$
$$U_b = R_s i_b + L_s \frac{di_b}{dt} + \frac{2S_b - (S_a + S_c)}{3} * U_{DC} \quad (12)$$
$$U_c = R_s i_c + L_s \frac{di_c}{dt} + \frac{2S_c - (S_a + S_b)}{3} * U_{DC} \quad (13)$$

To fully specify the system dynamics, the DC-side of the 3-phase PWM rectifier is represented using Kirchhoff's current law as:

$$i_{DC} = i_C + i_{load} \quad (14)$$
$$C\frac{du_{DC}}{dt} = S_a i_a + S_b i_b + S_c i_c - i_{load} \quad (15)$$

where i_{DC}, i_{Load}, and i_c are the total DC-bus current provided by the rectifier, the DC current on the load-side, and the capacitor current, respectively.

So, the combination of the above equations can be visualized in the form of a block diagram, representing the mathematical model of the input stage AFE PWM rectifier in a stationary abc frame system, as depicted in Fig. 6 [35].

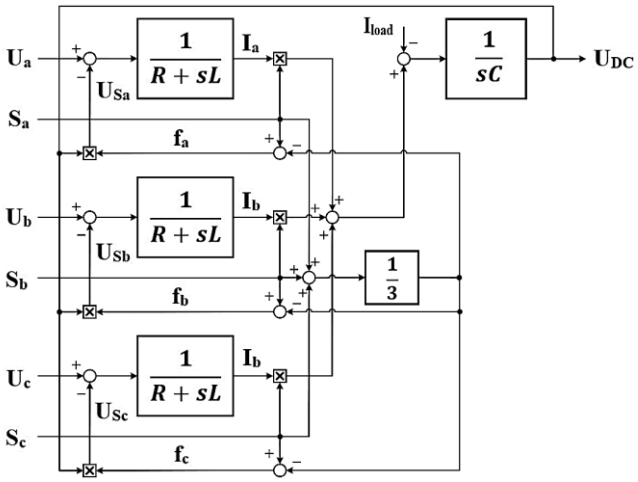


Fig. 6. Block diagram of a PWM rectifier in a stationary abc frame [35].

Since a 3-phase AC grid is expressed as a differential equation with time-varying characteristics as shown in Eqs. (1) to (3), it is difficult to control [37]. Therefore, if the coordinate conversion technique is applied and the 3-phase grid voltages and line currents are represented in a similar frame known as a dq synchronous frame, which revolves at an angular velocity ω ($\omega=2\pi f$ and f is the grid frequency), the time-varying coefficient is removed and converted into a time-invariant differential equation with constant coefficients (linear model), simplifying the analysis and control of the AFE PWM rectifier [38], [39]. The fundamental relation between vectors of the PWM rectifier in different coordinate frames is depicted in Fig. 7 [35], [40].

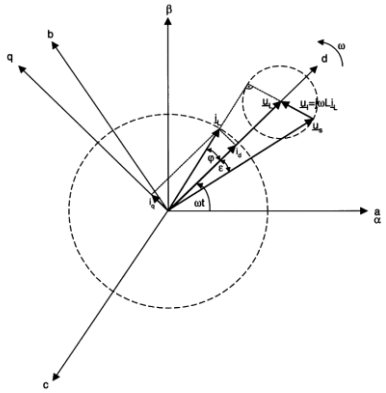


Fig. 7. Relation between vectors in a PWM rectifier [35], [40].

The transformation to the dq synchronous rotating frame from the abc stationary frame is comprehensively elucidated in [41], and therefore, it is not illustrated here. In that frame, the Eqs. (1) to (3) and (15) that describe the mathematical model of the PWM rectifier could be represented as [35]:

$$u_{Ld} = R_s i_{Ld} + L_s \frac{di_{Ld}}{dt} - \omega L_s i_{Lq} + u_{Sd} \quad (16)$$

$$u_{Lq} = R_s i_{Lq} + L_s \frac{di_{Lq}}{dt} + \omega L_s i_{Ld} + u_{Sq} \quad (17)$$

$$C \frac{du_{DC}}{dt} = \frac{3}{2}\left(S_d i_{Ld} + S_q i_{Lq}\right) - i_{load} \quad (18)$$

where u_{Ld}, u_{Lq}, and i_{Ld}, i_{Lq} are grid voltages and currents in synchronously rotating dq coordinates, respectively. The input voltages to the rectifier are u_{Sd} and u_{Sq}, the switching states in the synchronously rotating dq coordinate are S_d and S_q, and the angular velocity is ω.

Based on the dq transformations, the active and reactive powers taken by the proposed FC in that frame are expressed through Eqs. (19) and (20) [42].

$$P = \frac{3}{2}\left(u_{Ld} i_{Ld} + u_{Lq} i_{Lq}\right) \quad (19)$$

$$Q = \frac{3}{2}\left(u_{Ld} i_{Lq} - u_{Lq} i_{Ld}\right) \quad (20)$$

3.1.3. *Input stage control system*

The input stage control system of the proposed FC must meet several objectives, which are summarized as follows:

1. Regulate the DC-bus voltage to a predefined voltage value.
2. Ensure that the AC input currents have a waveform that closely resembles a sinusoidal wave and are synchronized in-phase with the AC voltages to get UPF.

3.1.3.1. *Grid synchronization*

Conventional PWM rectifiers use the zero-crossing technique to find the grid voltage phase, but if the grid voltage is not accurately measured for reasons such as harmonics or noise, the phase angle is not properly detected, making the control of the rectifier unstable. Therefore, in order to quickly and accurately get the phase of the grid voltage for synchronizing a PWM rectifier with a grid, the Phase-Locked-Loop (PLL) technique is applied in this paper [43]. Figure 8 illustrates the PLL block diagram.

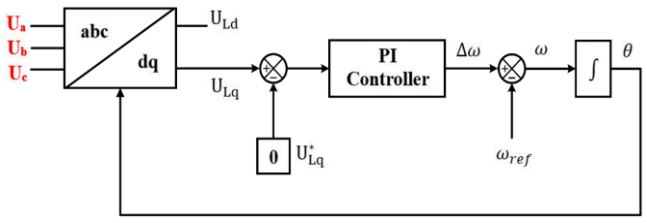


Fig. 8. PLL block diagram.

3.1.3.2. *Control strategy*

The VOC scheme is considered the most common control strategy, utilizing highly efficient dq-coordinate control systems to fulfill the growing demands for enhancing power quality [44], [45]. This strategy enables active and reactive powers to be independently managed by controlling the line current components within the synchronous dq frame [46]. For these reasons, VOC is the proposed control scheme adopted in the input stage of the considered FC. The VOC scheme is a cascaded closed-loop control structure that includes two control tiers, one for inner current control and the other for outer voltage regulation. By employing this control approach, it becomes feasible to control both the PF and the DC-bus output voltage simultaneously. Figure 9 illustrates the block diagram of the VOC strategy for the AFE PWM rectifier [47]. The inner control loops are utilized to control the direct (d) and quadrature (q) axis currents to fulfill the UPF condition by maintaining no phase difference between the grid voltage and the current [48]. Meanwhile, the outer control loop is responsible for maintaining a regulated DC-bus voltage and generating a reference current for the d-axis current controller [49]. In the VOC, fast transient response, high dynamic performance, and robust static performance are ensured using inner current control loops [50].

Figure 9 illustrates that the voltage-oriented dq-coordinate system splits the line current vector i_L into two orthogonal components, which are denoted as $i_L = [i_{Ld}, i_{Lq}]$. The component i_{Ld} manages the flow of active power, while i_{Lq} determines reactive power. Therefore, it is possible to manage both active and reactive powers separately, as mentioned earlier. The d-axis reference current i^*_{Ld} is determined by the DC-bus voltage controller, governing the active power exchange between the DC-bus and grid. Meanwhile, the q-axis reference current i^*_{Lq} is consistently maintained at zero for UPF control. The condition for UPF is fulfilled through alignment between the line voltage vector u_L and the line current vector i_L.

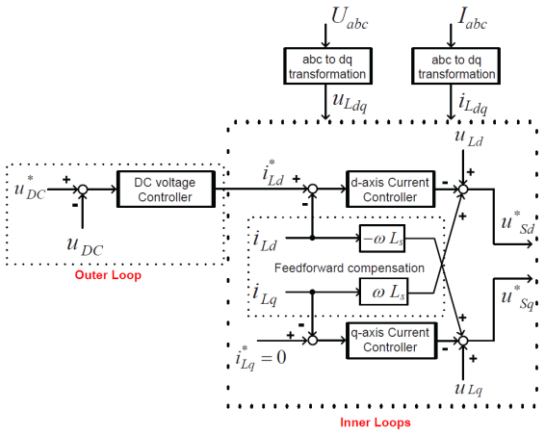


Fig. 9. Block diagram of the VOC controller for the AFE PWM rectifier [47].

As shown in Eqs. (16) and (17), the d-axis and the q-axis currents i_{Lq} and i_{Ld} are mutually coupled with the $\omega L_s i_{Ld}$ and $\omega L_s i_{Lq}$ parts. This signifies that controlling one of them will

result in a corresponding change for the other [51]. Consequently, achieving independent control of these currents isn't feasible in this case. Hence, to achieve independent control of these currents, it is essential to employ a decoupling control mechanism, as depicted in Figure 9. A feed-forward decoupling control approach is used. By rearranging Eqs. (16) and (17) to determine the terms of the voltage drop on the inductance L_s to control the line current i_L, the following equations become as:

$$u_{Sd} = u_{Ld} + \omega L_s i_{Lq} - \left(R_s i_{Ld} + L_s \frac{di_{Ld}}{dt}\right) \quad (21)$$

$$u_{Sq} = u_{Lq} - \omega L_s i_{Ld} - \left(R_s i_{Lq} + L_s \frac{di_{Lq}}{dt}\right) \quad (22)$$

Linear control techniques, like proportional integral (PI) controllers, find widespread use in the VOC scheme control loops because of their adaptability for tuning, simple structure, and practical implementation convenience. A PI controller is employed to control the DC-bus voltage in the outer loop, generating the d-axis reference current value. Meanwhile, two additional sets of PI controllers are utilized to regulate the source current in the inner loops, ensuring the d and q axis currents are regulated as needed.

A) Inner Current Control Loops

Regulating both active and reactive currents, i_{Ld} and i_{Lq}, respectively, is primarily the goal of two PI controllers in the inner current control loops. The d-axis current control loop is used for tracking the reference current value i^*_{Ld} obtained from the outer voltage control loop, while it is necessary to set the q-axis current i^*_{Lq} equal to zero to achieve the UPF condition. So, the output signals of the PI current controllers, corresponding to them, can be represented as new variables u'_{Sq} and u'_{Sd}. To achieve the specified current value of either i^*_{Ld} or i^*_{Lq}, the voltage needed to be applied across the line inductance is indicated by these variables. This makes it possible to formulate and control the new dynamic equations as follows [52]:

$$u'_{Sd} = R_s i_{Ld} + L_s \frac{di_{Ld}}{dt} \quad (23)$$

$$u'_{Sq} = R_s i_{Lq} + L_s \frac{di_{Lq}}{dt} \quad (24)$$

Equations (23) and (24) illustrate the complete independence of the two-axis currents, as u'_{Sd} is solely linked to i_{Ld} and u'_{Sq} is exclusively associated with i_{Lq}. To obtain reference signals u^*_{Sd} and u^*_{Sq} for the rectifier voltages, which are subsequently converted into 3-phase values that will be used with the modulation technique, feed-forward terms and the grid voltages, u_{Ld} and u_{Lq}, are incorporated with the controller output [35], [53], as shown in Eqs. (25) and (26).

$$u^*_{Sd} = u_{Ld} + \omega L_s i_{Lq} - u'_{Sd} \quad (25)$$

$$u^*_{Sq} = u_{Lq} - \omega L_s i_{Ld} - u'_{Sq} \quad (26)$$

where u'_{Sq} and u'_{Sd} represent the output signals of the current controllers.

The output signals of the PI current controllers, u'_{Sq} and u'_{Sd}, are represented as:

$$u'_{Sd} = K_{iP}(i^*_{Ld} - i_{Ld}) + K_{iI}\int (i^*_{Ld} - i_{Ld})\, dt \quad (27)$$

$$u'_{Sq} = K_{iP}(i^*_{Lq} - i_{Lq}) + K_{iI}\int (i^*_{Lq} - i_{Lq})\, dt \quad (28)$$

By substituting Eqs. (27) and (28) into Eqs. (25) and (26), correspondingly, the inner current control loops using two PI controllers become, as shown in Fig. 9.

$$u^*_{Sd} = -\left(K_{iP} + \frac{K_{iI}}{s}\right)(i^*_{Ld} - i_{Ld}) + \omega L_s i_{Lq} + u_{Ld} \quad (29)$$

$$u^*_{Sq} = -\left(K_{iP} + \frac{K_{iI}}{s}\right)(i^*_{Lq} - i_{Lq}) + \omega L_s i_{Ld} + u_{Lq} \quad (30)$$

B) Outer Voltage Control Loop

The outer voltage control loop utilizes a PI controller to guarantee that the DC-bus voltage remains at the required voltage reference, as depicted in Fig. 9. Then, the d-axis current reference value i^*_{Ld} is produced as the PI controller's output, as shown in Eqs. (31) and (32).

$$i^*_{Lq} = \left(K_{uP} + \frac{K_{uI}}{S}\right)(U^*_{DC} - U_{DC}) \quad (31)$$

$$i^*_{Lq} = K_{uP}(U^*_{DC} - U_{DC}) + K_{uI}\int (U^*_{DC} - U_{DC})\, dt \quad (32)$$

C) Active and Reactive Powers

Now, to achieve UPF operation with the AFE PWM rectifier where there is no need for reactive power, it's essential to either set $Q = 0$ or $i^*_{Lq} = 0$. By referring to the power equations outlined in Eqs. (19) and (20), it is possible to designate the reference value i^*_{Lq} as zero. It will lead to the alignment between the d-axis current and the grid voltage vector, thus resulting in $u_{Lq} = 0$. This results in a simplification in the equations for active and reactive powers, representing them as indicated in Eqs. (33) and (34).

$$P = \frac{3}{2} u_{Ld} i_{Ld} \quad (33)$$

$$Q = 0 \quad (34)$$

3.1.4. Design considerations for the input stage

3.1.4.1. Minimum DC-bus voltage

To achieve undistorted current waveforms, there is a need for the correct selection of the minimum DC-bus voltage, ensuring that the PWM rectifier operates effectively. Additionally, for fully rectifier control, it is essential to polarize its six diodes in the inverse mode under all AC voltage supply values. Consequently, to ensure that the diodes are in a blocked state, it is necessary to maintain a DC-bus voltage exceeding the peak DC voltage produced by the diodes themselves while also adhering to the rectifier's operational limits. Theoretically, for a diode rectifier, the highest achievable DC voltage at the output equals the peak value of the line-to-line RMS voltage, as shown in Eq. (35) [54].

$$U_{DCmin} > \sqrt{2}U_{LL(rms)} = \sqrt{2} * \sqrt{3} * U_{LN(rms)} = 2.45 * U_{LN(rms)} \quad (35)$$

Selecting a DC-bus voltage, that is approximately 15-20% greater than $\sqrt{2}U_{LL}$, is advisable [35]. Figure 10 illustrates the DC-bus voltage condition between the diode rectifier and PWM rectifier minimum limit. The previous voltage $U_{LL(rms)}$ equals the rectifier voltage U_s when the line impedance isn't considered. However, if the line impedance isn't considered ($R=0\Omega$, $L=0H$), Eq. (35) can be reformulated using the peak amplitude of the supply voltage E_m in the following manner:

$$U_{DCmin} > \sqrt{2} * \sqrt{3} * U_{LN(rms)} = \sqrt{3} * E_m \quad (36)$$

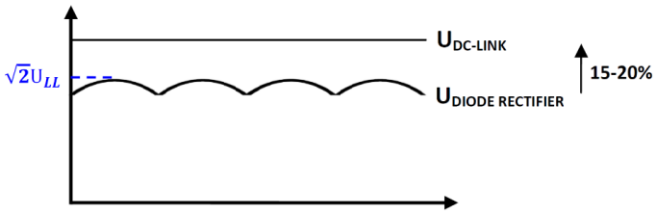


Fig. 10. DC-bus voltage condition.

The DC-bus voltage is contingent on the specific PWM technique being utilized. The Sinusoidal pulse width modulation (SPWM) technique is adopted in this paper, A triangular wave with a constant frequency and amplitude is compared to the 3-phase reference voltages. In this scenario, the maximum reference voltage will be $\frac{U_{DC}}{2}$ as shown in Fig. 11 [55].

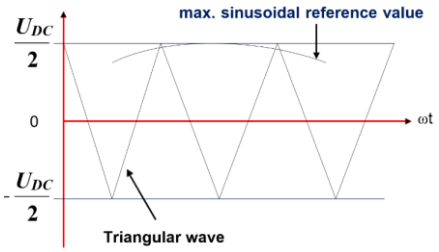


Fig. 11. Maximum sinusoidal voltage reference for SPWM [55].

Ultimately, the minimum DC-link voltage will be:

$$U_{LN(peak)} = \frac{U_{DC}}{2} \quad (37)$$

$$\frac{U_{LL(rms)}}{\sqrt{3}}\sqrt{2} = \frac{U_{DC}}{2} \quad (38)$$

$$U_{DCmin} > 2U_{LN(peak)} = \frac{2\sqrt{2}}{\sqrt{3}} * U_{LL(rms)} = 1.663 * U_{LL(rms)} \quad (39)$$

3.1.4.2. Line inductance

Proper design of the line inductor is crucial, as a low inductance value can result in significant current ripple and increased reliance on the line impedance in the overall design. While increasing the inductance value will indeed reduce the current ripple, it may also limit the rectifier operational range. It is considered that the inductance's voltage drop is responsible for regulating the current. The rectifier voltage has an effect on this voltage drop, but the DC-bus voltage determines its maximum limit. Hence, a low inductance or a high DC-bus voltage are necessary to achieve a high current through the inductor. The DC-bus voltage should be raised to a level that compensates for the voltage drop across the inductance. According to [35], [54], the line inductance is considered when calculating the minimum DC-bus voltage. When the inductance value is zero, the formula below will match Eq. (36).

$$U_{DC} > \sqrt{3[E_m^2 + (\omega L_s i_{Ld})^2]} \quad (40)$$

Finally, the equation mentioned above is utilized to determine the limit of inductance. Therefore, the maximum inductance can be written as:

$$L_s < \frac{\sqrt{\frac{U_{DC}^2}{3} - E_m^2}}{\omega i_{Ld}} \quad (41)$$

Hence, Fig. 12 depicts the block diagram for the input stage of the proposed FC. The complete block diagram

contains the forward path, the feed-forward path, and the feedback path, thus constituting a dual closed-loop system. The forward path means that the AC power goes from the grid through line input filters, an AFE PWM rectifier, and a DC-bus capacitor, facilitated by SPWM signal generation, ultimately reaching the output stage. The feed-forward path commences with the measurement of 3-phase input voltages and currents to the VOC controller through the abc-to-dq transformation. The feedback path monitors and measures the DC-bus voltage, compares it against the reference DC voltage, and then sends the error signal back to the VOC block. The output of the VOC controller is converted again into abc components. Then, the SPWM generation block is then provided with these abc components to generate gating pulses for the six IGBTs. These gating pulses are responsible for controlling the switching of IGBTs, ensuring that the AFE rectifier achieves UPF and sinusoidal input current.

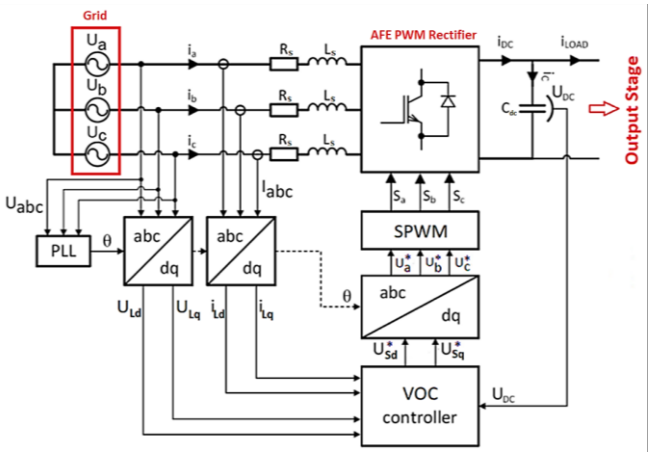


Fig. 12. Block diagram for the input stage of the proposed FC.

3.2. Output Power Stage (DC-DC)

Since the high DC-bus voltage provided by the boost-type rectifier in the input stage of the proposed FC can't be directly employed for charging the EV battery. Hence, the output stage adopted in this paper comprises a buck converter designed to make this high voltage compatible with the EV battery voltage. Moreover, it controls the process of battery charging to extend battery longevity, minimize heat generation, and so on.

3.2.1. Circuit description and operating analysis

The DC-DC buck converter can lower the DC-bus voltage while simultaneously increasing the DC-bus current to a higher level at the battery side [56]. A typical DC-DC buck converter includes a diode, a switching device that operates in buck mode, and a capacitor and inductor. The capacitor and inductor serve as a low-pass filter to dampen the rapid switching of the electronic switch, resulting in a stable and smoothed output DC voltage. The diode has a critical function in ensuring that the inductor current flows in the desired direction when the switching device is open. Figure 13 depicts a schematic representation of the buck converter adopted in the output stage.

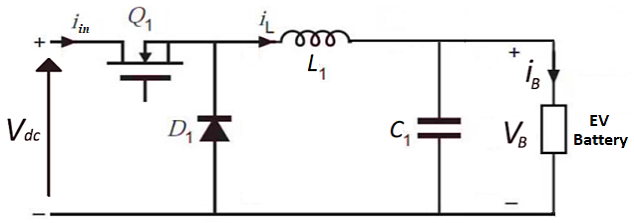


Fig. 13. Buck converter in the output stage of the proposed FC.

The equations that govern the output stage are presented below [57]:

$$V_{dc} = V_B + L_1 \frac{di_L}{dt} \tag{42}$$

$$i_B = i_L + C_1 \frac{dV_B}{dt} \tag{43}$$

Considering Fig. 13, current passes to the battery from the DC-bus via the inductor and capacitor during the ON state of the electronic switch. Then the inductor current I_L rises in tandem with the increase in the electronic switch current I_{in}. In particular, the inductor retains a portion of the current during the ON state time (DT) when the electronic switch is closed, and the remaining current is then released to both the capacitor and the battery. The change in inductor current as the switching device closes is described by Eq. (44).

$$(\Delta I_L)_{closed} = \left(\frac{V_{dc} - V_B}{L_1}\right) DT \tag{44}$$

While at time (1-DT), the switching device is in the OFF state, so the DC-bus V_{dc} can't supply current. The battery takes current from the inductor, leading to a linear decrease in the current within the inductor. The change in the inductor current as the switching device opens is formulated in Eq. (45).

$$(\Delta I_L)_{open} = -\frac{V_B}{L_1}(1 - D)T \tag{45}$$

Under steady state condition, the total inductor current comprises the current as the switching device closes and the current as the switching device opens, resulting in Eqs. (46) and (47).

$$(\Delta I_L)_{closed} + (\Delta I_L)_{open} = 0 \tag{46}$$

$$\left(\frac{V_{dc} - V_B}{L_1}\right) DT - \frac{V_B}{L_1}(1 - D)T = 0 \tag{47}$$

Simplifying Eq. (47) yields the relation between the battery and DC-bus voltages at a given duty cycle D, as shown in Eq. (48). It is observed that the battery voltage V_B is always lower than the DC-bus voltage V_{dc}. The waveforms of the buck converter are depicted in Fig. 14.

$$V_B = DV_{dc} \tag{48}$$

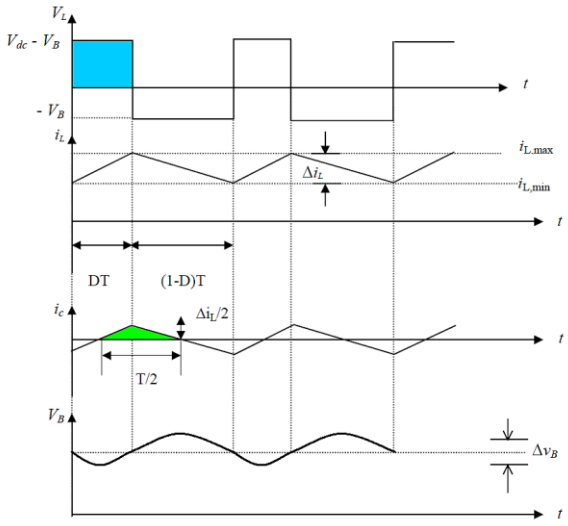


Fig. 14. Buck converter waveforms.

The inductor and capacitor selection equations, as per [58], are provided below:

$$L_1 = \frac{V_B(V_{dc} - V_B)}{f_{swo} * V_{dc} * \Delta I_L} \tag{49}$$

$$C_1 = \frac{\Delta I_L}{8 * f_{swo} * \Delta V_B} \tag{50}$$

where V_{dc} represents the DC-bus voltage, V_B represents the battery voltage, ΔI_L represents the peak-to-peak current ripple of the inductor, ΔV_B represents the peak-to-peak voltage ripple of the battery, and f represents the switching frequency.

3.2.2. Charging method

The output stage requires different modes of control to ensure safe battery charging by employing an appropriate charging method. Commercially available DC FCs typically utilize the CC-CV charging method [59]. Figure 15 shows the charging curves for the CC-CV method. The battery voltage rises in direct proportion to the state of charge (SOC) during the CC phase. Upon entering the CV phase, the charging current supplied to the battery gradually diminishes.

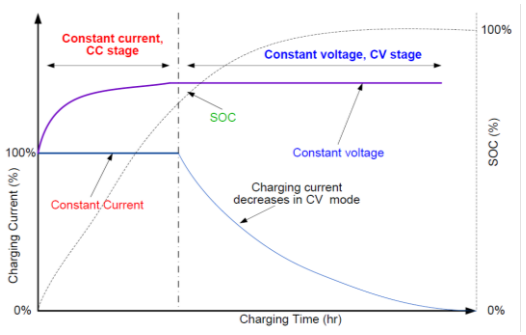


Fig. 15. Charging curves for the CC-CV method.

The battery charging method in this paper adopts a two-stage CC-CV method, which consists of a CC phase followed by a transition to a CV phase. During the CC phase, the goal is to provide the maximum current, often called the bulk current, to the battery until it reaches a SOC of approximately 80% as rapidly as feasible, then it transitions to the CV phase. Once in the CV phase, the objective is to uphold the battery voltage at a specific DC threshold value, typically matching the battery's open circuit voltage (OCV) [60]. Throughout this phase, the current continues to flow depending on the voltage difference till the SOC becomes 100%, indicating that the battery has reached full charge. The basic control mechanism of the CC-CV charging phases adopted in this paper is illustrated in Fig. 16.

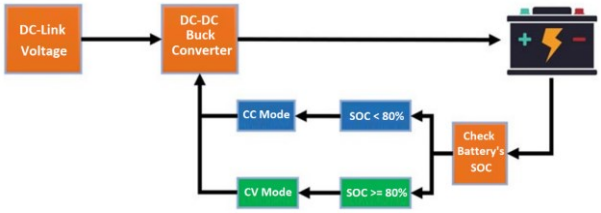


Fig. 16. Control mechanism of CC-CV charging phases adopted in this paper.

Hence, Fig. 17 depicts the block diagram for the output stage of the proposed FC. The charging method is executed within the battery charging control system through the utilization of two distinct closed-loop systems, each utilizing a PI controller. These two loops consist of the current and voltage control loops, with the ultimate goal of achieving fast-charging. During the initial charging mode, the battery undergoes charging with a constant current under the supervision of the current control loop till the battery SOC attains 80%. Moving to the subsequent mode, the battery charging process employs a constant voltage under the supervision of the voltage control loop till the SOC becomes 100%.

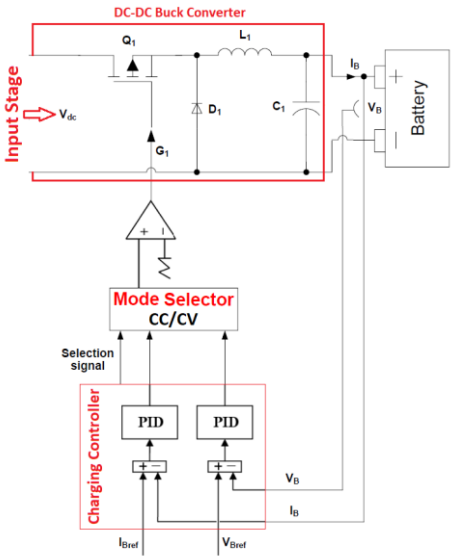


Fig. 17. The block diagram for the output stage of the proposed FC.

After integrating both the input and output stages with their control strategies, the overall representation of the proposed FC connected to the AC grid with a structural control scheme is illustrated in Fig. 18. Within the input stage, a VOC controller is employed in conjunction with the SPWM technique to guarantee a stable DC-bus voltage to the buck converter while mitigating the introduction of harmonics into the grid. In particular, the outer control loop controls the output DC-bus voltage U_{DC} to match its reference $U_{DC_{ref}}$ and produces the reference of the active current $i_{Ld_{ref}}$. Meanwhile, the inner control loops are employed to attain the UPF condition. To achieve that, the reactive reference current is adjusted to zero ($i_{Lq_{ref}} = 0$). While, in the output stage, the current control loop is set up to keep the battery current I_B at the desired value I_{Bref} during the CC phase. In contrast, the voltage control loop is structured to ensure that the battery voltage V_B closely follows the reference voltage V_{Bref} during the CV phase.

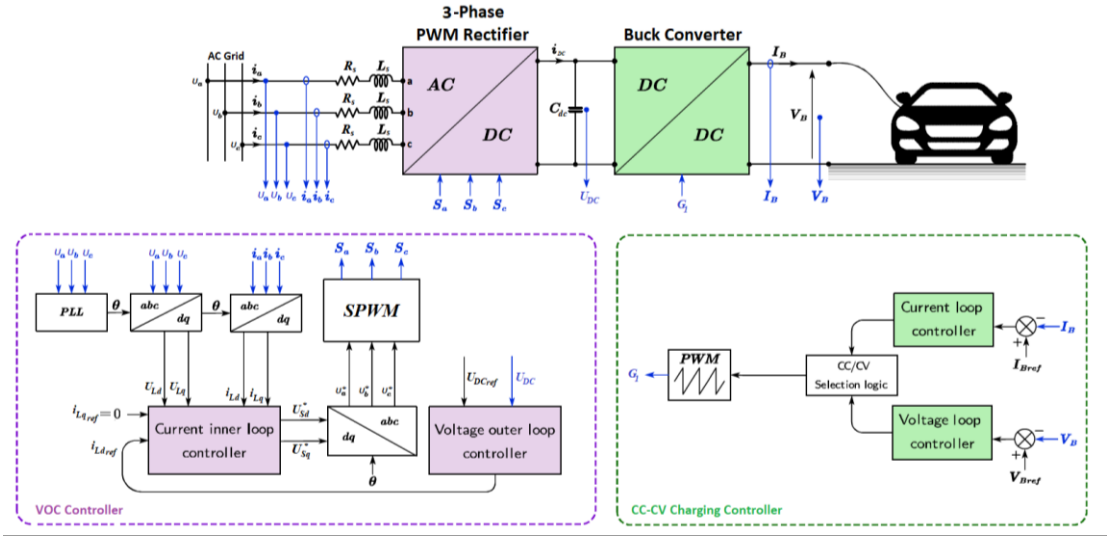


Fig. 18. The overall representation of the proposed FC with a structural control scheme.

4. Simulation Results

To assess the performance of the FC configuration and proposed control strategy, a 50-kW FC has been simulated using the MATLAB/Simulink® software environment. The system is modeled and controlled using the power electronic modules provided by MATLAB. Figure 19 illustrates the complete simulation model of the proposed FC. The FC is designed to draw power from a 3-phase 380 V_{AC}, 50 Hz grid. The input stage includes an AFE PWM rectifier that transforms the 380 V_{AC} grid voltage into a 650 V_{DC} DC-bus voltage. The gating signals for the rectifier switches are produced utilizing the SPWM technique to attain high PF and reduce THD while maintaining a regulated DC-bus voltage. This regulated DC-bus voltage is provided directly to the output stage. Subsequently, the output stage, which comprises a buck converter, transforms this DC voltage into the battery voltage to facilitate charging. The FC is designed to charge a 360 V_{DC}, 65 Ah lithium-ion batteries, with a maximum charging current capped at 130 A in our case. The design specifications mandate a maximum output voltage of 375 V_{DC}. The entire system employs a switching frequency of 20 kHz to ensure a compact design while maintaining high efficiency. The VOC, adopted in the input stage, controls the power flow of the 3-phase PWM rectifier, while the CC-CV, adopted in the output stage, regulates the battery charging. Table 1 gives the system parameters utilized in the simulation model. The desired operational performance can be achieved using the PI controller parameters outlined in Table 2.

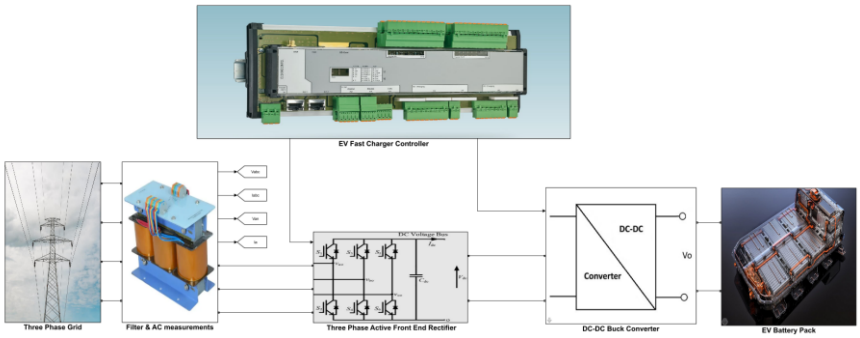


Fig. 19. Simulation model of the proposed FC.

Table 1. Proposed FC parameters for simulation

FC specifications			
Parameter		**Value**	
Rated power, P		50 kW	
Grid input voltage, U_{LL}		3-phase, 380 V_{AC}	
Grid frequency, f		50 Hz	
Power factor, PF		More than 99%	
Total harmonic distortion, THD		< 5%	
EV battery pack		360 V, 65 Ah lithium-ion battery	
Output DC voltage, V_B		360 – 375 V	
Maximum output DC current, I_B		130 A	
Fast-charging method		CC-CV	
Input stage parameters		**Output stage parameters**	
Parameter	**Value**	**Parameter**	**Value**
Input filter inductance, L_s	4 mH	Converter inductance, L_1	20 mH
Input filter parasitic resistance, R_s	0.1 Ω	Converter capacitance, C_1	100 µF
DC-bus capacitor, C_{dc}	1000 µF	Converter switching frequency, f_{swo}	20 kHz
DC-bus voltage, U_{DC}	650 V	Output current ripple, ΔI_B	< 1%
Rectifier switching frequency, f_{swi}	20 kHz	Output voltage ripple, ΔV_B	< 1%
DC-bus voltage ripple, ΔU_{DC}	< 1%		

Table 2. PI-controller design parameters

PI Controller	**K_p**	**K_i**	**K_d**
Input Stage			
Current	2000	100	0
Voltage	0.4	160	0
PLL	180	3200	1
Output Stage			
Current	0.3	2.25	0
Voltage	0.9	2350	0

A series of simulation results are conducted to analyze the FC, which are presented below. Figure 20 shows the simulation waveform for the dynamic response of the input stage performance concerning grid voltage and the associated current for a particular phase during the battery fast-charging process. Both the grid voltage and current remain in-phase, indicating a UPF throughout the CC and CV charging phases. Moreover, the grid current exhibits a perfectly pristine sinusoidal waveform, ensuring that the grid remains unpolluted by the FC. Hence, it can be stated that the dynamic performance is satisfactory throughout the CC-CV fast-charging process.

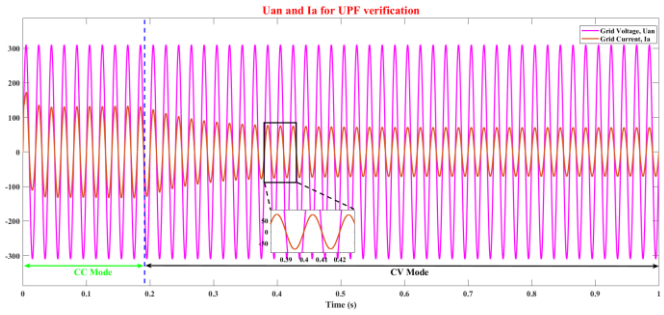


Fig. 20. Input stage performance throughout the CC-CV fast-charging process under UPF.

Figure 21 presents the simulation waveform depicting the regulation of the DC-bus voltage in the input stage. The DC-bus voltage has been well regulated to a reference voltage of 650 V_{DC} without any steady-state error and under 1% ripple. Furthermore, it's noticed that the DC-bus voltage demonstrates an excellent dynamic response despite fluctuations during the initial transient condition. Even when the charging mode changes, it tracks the reference voltage quickly within a period of approximately 0.05 sec. The DC-bus voltage ripple ranges within ±1 V around the reference value.

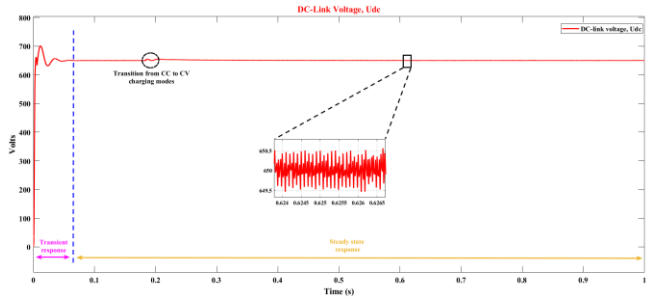


Fig. 21. DC-bus voltage regulation.

In order to emphasize the benefits of the proposed FC, Fig. 22 depicts the harmonic analysis of grid input current for one phase, calculated by using MATLAB software. This shows that the THD in grid input current is only 1.60%, which is well below 5%, satisfying the regulations set in IEEE-519, which means that the impact on the entire grid and other devices due to harmonics is lower.

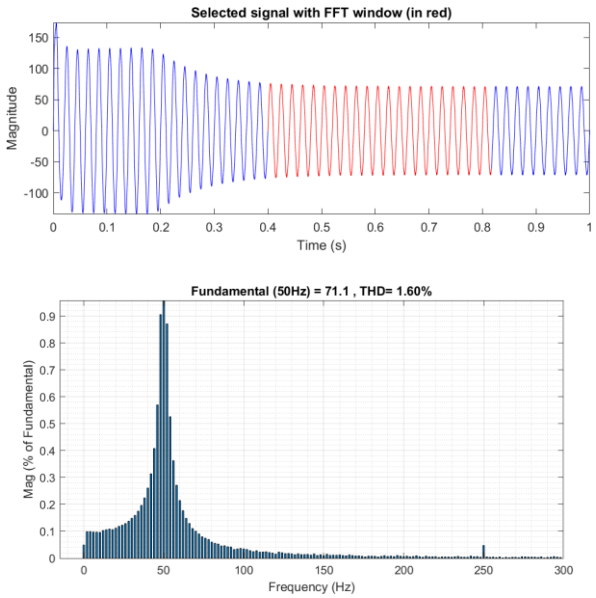


Fig. 22. Harmonic analysis of the grid input current.

Figure 23 shows simulation waveforms for the output stage performance during CC-CV charging modes. As seen from this figure, the CC phase represents the initial charging phase, with the battery being charged at a rated current of 130 A. Consequently, in this phase, both the battery SOC and its voltage value increase. This CC charging process persists till the battery SOC reaches 80%; then, the battery charging mode shifts to the CV phase. During CV phase, the battery voltage maintains a consistent level of 374.5 V, and the charging current progressively decreases as the battery reaches its maximum capacity. The CV charging process will continue until the battery SOC reaches 100% or the charging current falls below the charging termination limit. It's worth noting the seamless transient response as well as the consistently stable operation in the steady state. Furthermore, the simulation waveforms provide confirmation that the fluctuation factor of both the output voltage and current are consistently kept below 1% of their respective nominal values, aligning with the specifications detailed in Table 1.

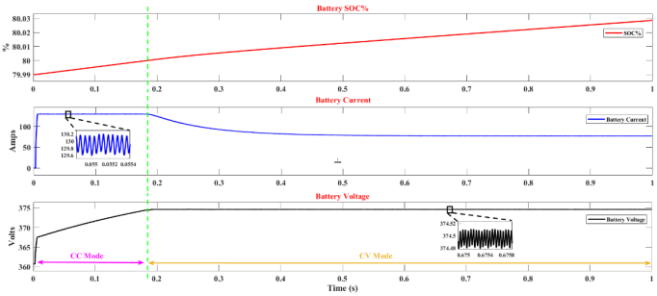


Fig. 23. Output stage performance during the CC-CV charging modes.

5. Conclusions

This paper proposes a grid-connected FC that is highly feasible for fast-charging applications in plug-in EVs. The proposed FC is based on a dual-stage configuration. The input stage incorporates an AFE PWM rectifier of the two-level type that achieves superior results in regard to THD and PF by complying with the grid codes. On the other hand, the output stage comprises a back-end buck converter responsible for delivering the appropriate voltage and current for battery charging. The FC system operates through a proposed control strategy that includes VOC scheme and CC-CV charging method, yielding outstanding performance.

The paper extensively elaborates on the operational analysis, modeling, and control of both the input and output stages, along with providing a comprehensive explanation of the proposed control strategy. The simulation results strongly support the effectiveness of the proposed control strategy, showing extremely promising results, including attaining a UPF, maintaining a THD of 1.6% according to the IEEE-519 standard, achieving good dynamic response, regulating the DC-bus voltage level with minimal ripple, and accomplishing CC-CV fast-charging with minimal ripple in both the battery current and voltage. Finally, the proposed FC comes with many desirable aspects, including a simple structure, well-established proposed control scheme, a streamlined power

conversion setup with fewer electronic components, inherent protection against reverse current from the battery, cost-effectiveness, and compactness.

Author Contributions

Mohamed Seleem was responsible for the conceptualization, validation, resources, data curation, software development, and project administration. Yousry Atia and Belal Abou-Zalam jointly contributed to the methodology, formal analysis, investigation, and original draft preparation. Sameh Abd-Elhaleem was responsible for the review and editing, visualization, supervision, and funding acquisition. All authors have read and agreed to the published version of the manuscript.

Conflict of Interest

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